

**2009**

PSAS/PSU ECE Capstone Report

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# Abstract

The Portland State Aerospace Society is a community based, educational project which focuses on the development of amateur rockets. Since PSAS was founded in 1998, the group has developed three different rockets, each undergoing design revisions as ideas changed and new technology became available. The current rocket under development by PSAS is named Launch Vehicle 2-c, or LV2c. As a result of the previous rocket, the LV2b, being destroyed after failure of its recovery system, the PSAS team has made several revisions to the rocket’s design. This has been not only to resolve the problem with the recovery system, but also to introduce some new technologies into the avionics systems of the LV2c. As a part of this process, PSAS has provided several aspects of the redesign as a project for Portland State University’s 2009 ECE Capstone Class.

The 2009 PSAS Capstone Project involved the redesign of two main components of the LV2c’s avionics systems. The first was the Generic Front End (GFE) which is installed on each of the separate avionics devices, also called nodes, and includes an ARM based microprocessor, highly available power supply (HAP), and switching power supply (SPS). The second was the Avionics Power System (APS) which is essentially responsible for the distribution of power and various data signals among each of the avionics nodes. This report details the functionality of the GFE and APS, the reasons for the redesigns, the design process, and the final products achieved by the 2009 PSAS Capstone Team.

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# 1 Introduction

### 1.1 About PSAS

The Portland State Aerospace Society, also known as PSAS, is a community based, ongoing educational project at Portland State University. The participants of this group include PSU students, faculty and staff, as well as members of the local community ranging from high school students to industry engineers.

The ultimate goal, and vision statement of PSAS is “to put nano-satellites into orbit.” As lofty a goal as this may be in terms of technical, logistical and financial requirements, such a goal ensures that the project as a whole is continually moving forward. Currently, PSAS is focusing on the first stage in completing this goal which is, “to develop an inexpensive, highly modular and actively guided sounding rocket.” A sounding rocket is a small to medium sized, suborbital vehicle capable of reaching extreme altitudes, but always falling back to Earth rather than entering orbit. Such rockets fall into the category of “amateur” rockets in that they are larger than the typical model rocket, but smaller than the commercial type. Though the rockets developed by PSAS are not the largest, and may not reach the highest altitudes, the hope is that they will be ranked among the most sophisticated.

The development of these rockets is comprised of four key areas. The first is the avionics system, which deals with the on-board electronics systems, and acts as the “brains” of the rocket. This includes the on-board computer, navigation, data collection and recovery systems. Next there is the airframe, which deals with the physical design of the rocket itself, and focuses on such items as the rocket’s frame, or skeleton, external skin and fins. The Propulsion system, of course, deals with the means by which the rocket will take flight. Finally, the ground system deals with the launch tower, launch control module, ground based communications, ground based software and logistical equipment.

The project which PSAS provided to Portland State University’s 2009 ECE Capstone class focused on redesigning several components of the avionics system of the current rocket design (LV2c). The details of this project are provided in the remainder of this report.

### 1.2 Project Background

Since their establishment in 1998, PSAS has designed and implemented several amateur rockets, which they call Launch Vehicles. With each new design, the technology utilized in the previous rockets is assessed and often updated according to past performance, introduction of new technology, and/or new design ideas. The LV2c rocket is an example of just such a revision.

The predecessor to the LV2c, aptly named the LV2b, was launched with a full avionics system on August 20th, 2005. Unfortunately, an unforeseen problem with the recovery node resulted in the parachutes failing to deploy, which in turn resulted in the destruction of the LV2b. Though this flight was considered a success in that the rest of the avionics systems functioned well, the recovery system failure led to a rigorous reassessment of all of the previous avionics systems’ designs. Out of this reassessment came not only ideas for redesign of certain avionics components, but also the addition of new avionics systems. It is at this point that PSAS utilized the 2009 ECE Capstone class to help in the redesign process.

Initially, the scope of the 2009 Capstone Project was divided into two separate parts, each designed for its own separate Capstone group. These were the redesign of the LV2b pyrotechnics node, the key component of the recovery system, and the addition of a new navigation sensor suite, respectively. It was decided, however, that PSAS did not have the resources to lead both groups separately and so the two projects, along with their respective groups, were combined into one large group and the overall scope of the new, single project was revised. The resulting project definition specified by PSAS was essentially to redesign two of the nodes from the LV2b avionics system. The task of redesigning the Pyrotechnic Node for the recovery system was kept, and in addition we were given the task of redesigning the rocket’s Avionics Power System, or APS. Each of these tasks would require the redesigning of several components, and thus these were further broken down into sub-tasks to be distributed among the Capstone Team. Below is a list of these sub-tasks for each of the nodes.

*Pyrotechnic Node Tasks:*

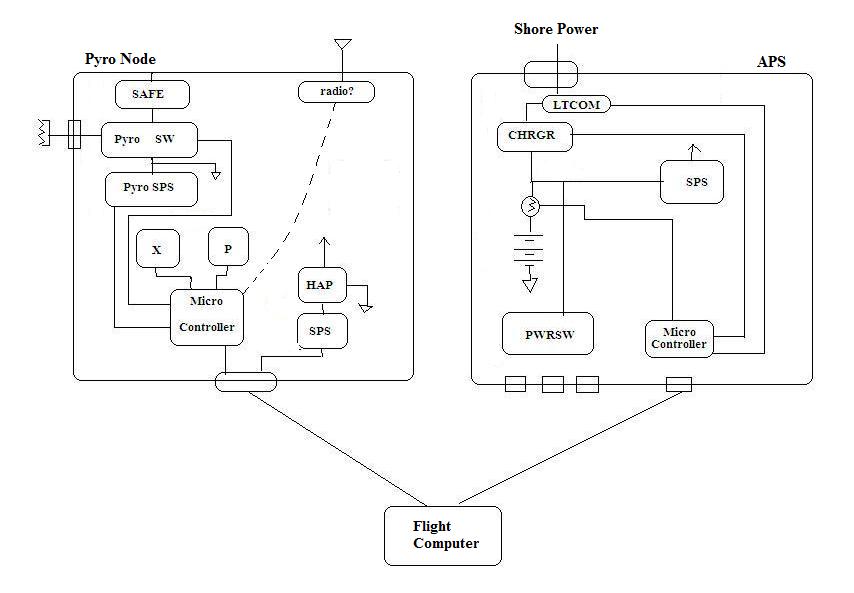
1. Update the SPS (switching power supply) from that which was implemented on LV2b. New design was to be modernized, built and tested
2. Update HAP (highly available power) for better system reliability
3. Redesign Pyro power supply (ignites charges which cause separation of rocket sections for recovery parachutes to deploy).
4. Sensors (barometer, accelerometer)
5. Redesign Pyrotechnic Node firmware (embedded program controlling Pyrotechnic Node)

*Avionics Power System Tasks*

1. Battery selection: includes review, testing and weight and volume considerations
2. Battery charger design
3. LTC communication interface: an umbilical connection that powers the rocket and charges the battery, as well as provides communication link between ground computer and avionics systems
4. Redesign power switches which control power distribution to other nodes
5. Redesign APS firmware

A block diagram of the two nodes described above is shown in figure 1 below. The figure serves to provide a graphical representation of each node to aid in the understanding of the above tasks.

Figure 1: Pyrotechnic Node and APS Node Block Diagram

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While the figure above does not provide a great deal of information about the details of component functionality, we get an idea as to how the components interact, which provides insight into the assigned tasks.

In the initial stages of this project, the task lists and the above figure were essentially all we were given before we were each assigned to our specific tasks. As such, over the first several weeks, each member of the Capstone Team spent the majority of their time researching their respective tasks. It soon became clear to our PSAS sponsors that re-prioritizing the tasks listed above so that each member of the group was essentially working on the same node would result in more productivity overall. As such it was decided that our focus as a team would be narrowed down further.

The revised scope of the project made the redesign of the Avionics Power System the main priority of this project. Also, as can be seen in the original task lists, as well as figure 1 above, the microcontroller and associated firmware, as well as the SPS and HAP are present on both nodes. In fact, it turns out that these components are present on every node implemented on the rocket. This being the case, these aspects of the original project scope were kept due to their importance to the entire avionics system of the rocket. The redesign of the Pyrotechnic Node was not completely eliminated; rather it simply became an aspect of the project to be dealt with only given enough time to do so.

This revision to the project scope left us with our final task list for the 2009 PSAS Capstone Project.

### 1.3 Project Overview

After the revisions described above, the 2009 PSAS Capstone Project consisted of the following tasks:

*Avionics System Generic Front End*:

* Switching Power Supply (SPS) design to provide 3.3V and 5V power to each node
* Highly Available Power (HAP) supply to provide battery backup to each node
* Microcontroller interfaces and communication

*Avionics Power System Node:*

* Select a new system battery
* Design a new battery charging system
* Design a system of sensors for battery monitoring and management
* Design power switch network to control distribution of battery power to other avionics nodes
* Select and design a new pressure sensing system
* Add a USB (Universal Serial Bus) Hub to APS board to distribute USB data to peripheral nodes

*Generic Node Firmware Development*

* Error handling
  + Error levels: debug, info, warn, error
  + Error logs (Sequential error list and error count)
  + Error messages (protocol undecided, may be CAN, UART, or USB)
* Serial console
  + Command interface
  + Communication interface to the error logs (request counts, etc)

*APS Node Firmware Development*

* APS must have states:
  + Sleep
  + Wake
  + Safe
  + Armed
    - Armed must check to see that all is in place for launch.

*Additional Firmware Development*

* Software to drive the rest of the APS Power System and Umbilical as time allows...

The remainder of this document provides an explanation of each of the items listed above, along with a description of the design process and final result for each. As it is present on all avionics nodes, the Generic Front End (GFE), and all related components are discussed first, followed by the Avionics Power System. Finally, the firmware development is detailed.

# 2 Generic Node Front End (GFE)

The Generic Node Front End (GFE) contains all the necessary hardware and firmware to handle communications to and from the flight computer as well as the other nodes. It will be found onboard all of the nodes in one form or another and will provide central processing and power delivery services to the electronics and sensors onboard the node. The basic node consists of four major areas, the switching Power Supply or SPS, the Highly Available Power Supply or HAP (onboard battery backup), the Microprocessor and associated interfacing, and finally the Node Specific Hardware. The update performed by this Capstone carries the GFE hardware from revision LV2B to LV2C. There are several reasons for this update. They include a need to see more interface capability from the microprocessor, resulting in a change from the LPC2148 to the LPC2368 microprocessor. There was also a desire for a power supply capable of delivering up to one amp on both the 5 and 3.3 volt rails resulting in an SPS update. In addition, the HAP is now integrated as an option for all nodes. The remainder of this GFE update section will detail specific operation of the three GFE sections.

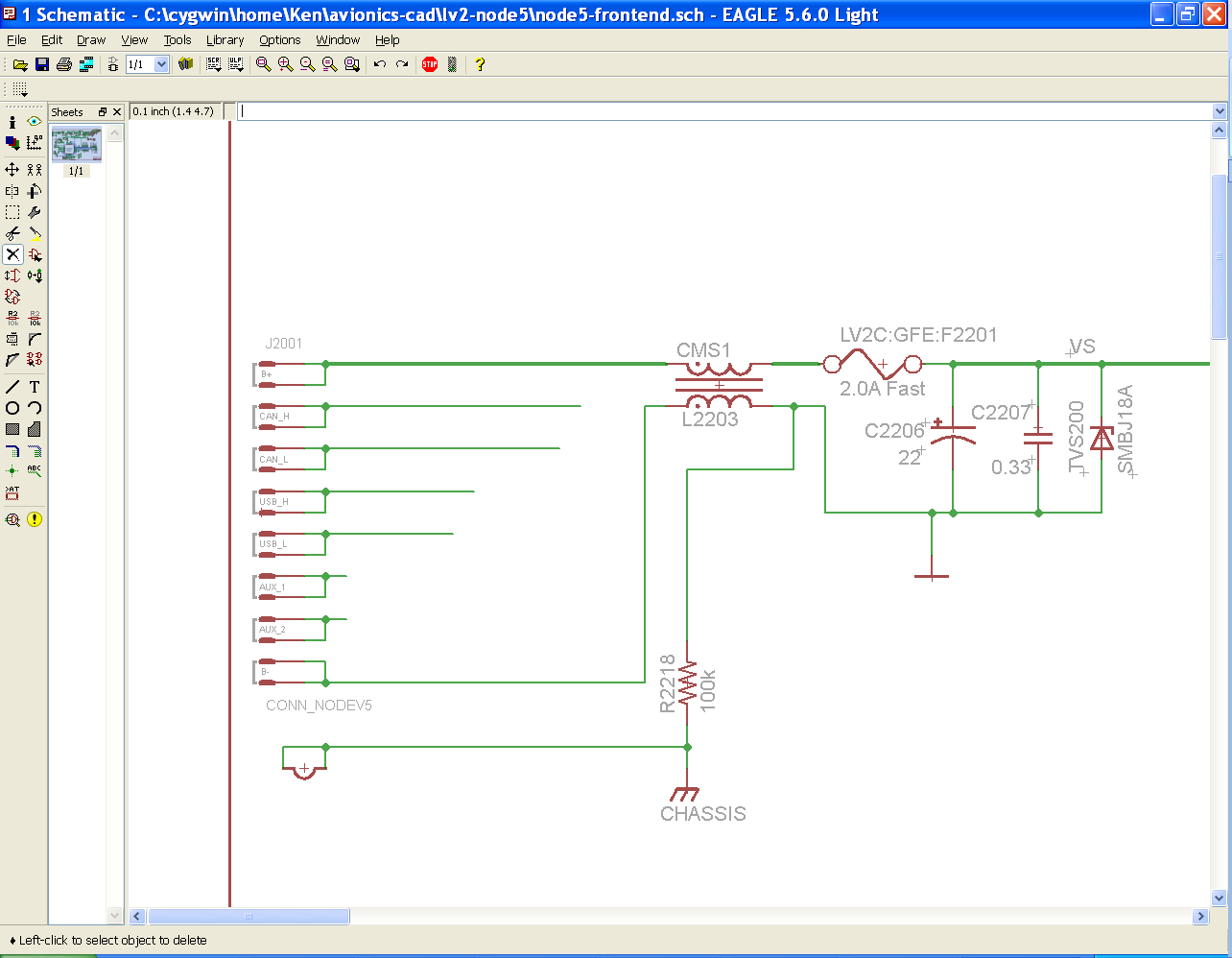
### 2.1 SPS

The Switching Power Supply performs the job of power delivery on all node circuit boards. The Avionics Power System (APS) delivers roughly 14.8 Volt DC power to the board through a 16 pin edge mounted connector. In addition to the power delivered, each connector distributes various data signal lines which will be described later. From the connector, power flow is through the Passive Protection Block, then through the Active Protection Block and into the actual SPS IC which is an LT3972 from Linear Technologies.

The SPS can be configured to deliver one of two output voltages. For nodes equipped with the HAP the output of the LT3972 is configured to output 5 volts DC and feeds the HAP charger and the HAP output regulator. For nodes not equipped with the HAP, the LT3972 can be configured for either 5V or 3.3V operation, and feeds power directly to the node devices. In many cases it will be desirable to provide both 5V and 3.3V power to a node, and this can be accomplished by configuring the LT3972 to deliver 5V, while populating the HAP output regulator to deliver the final 3.3V output to the circuit board. The 3.3V power line is almost always necessary given that the microprocessor is a 3.3V device.

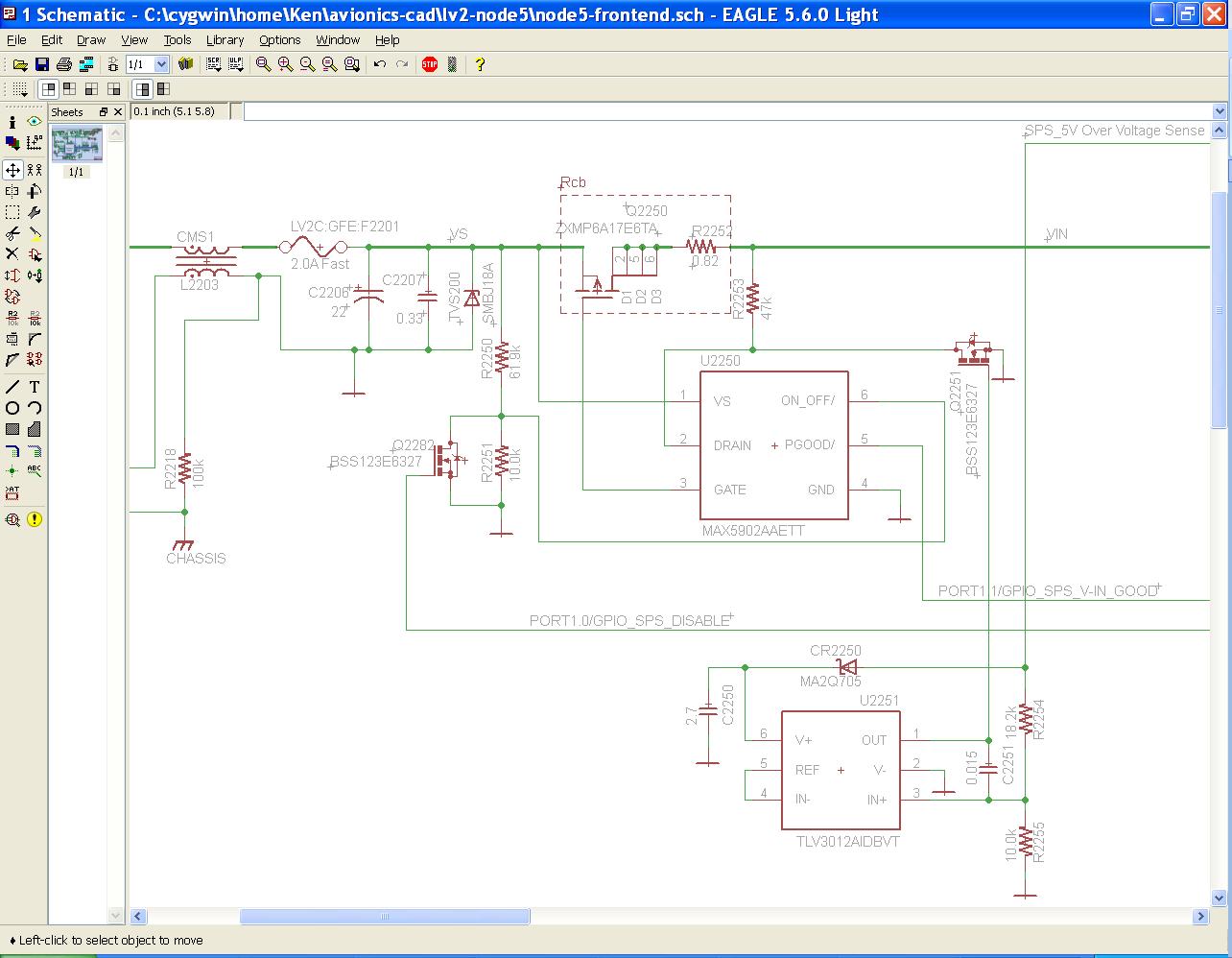
The following EAGLE drawing, shown in figure 2, details the frontend passive block, which is almost unchanged from the LV2b design. J2001 is the power connector that brings power into the board from the APS. L2203 is an EMI choke whose job is to cut down on RF noise that may be trying to couple in on the wires from the APS to the node. F2201 is a fuse set for 2 Amps. The fuse should be sized for the particular node in which it is used, though at 2 Amps, the circuitry on this board should be safe. C2206 and C2207 are there to provide additional high frequency filtering, while TVS2201 is a zener like device akin to a surge suppressor that is put in place to short power surges to ground. R2218 is the single point that connects the circuit board ground to the chassis ground.

Figure 2: GFE Passive Protection Block



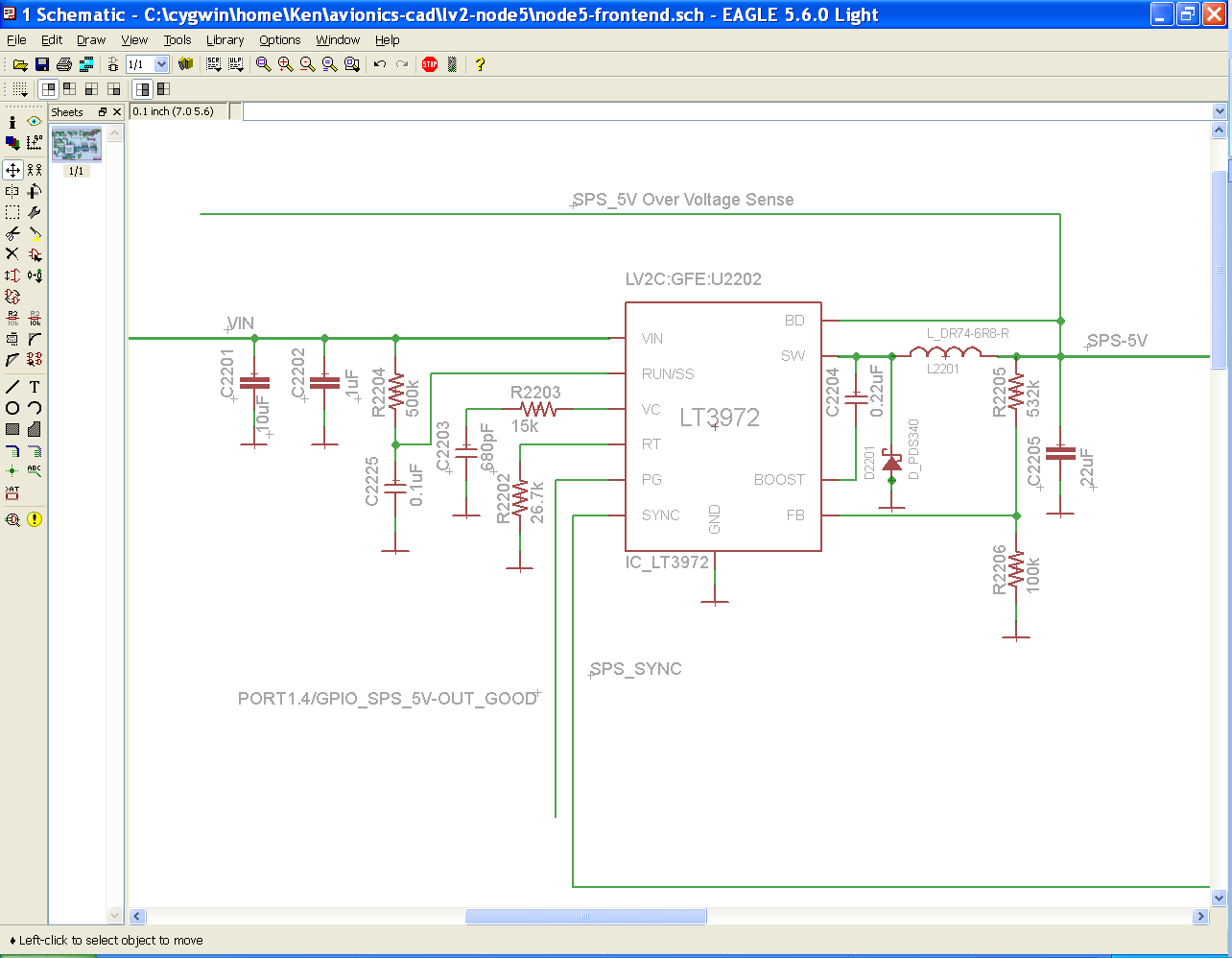
Following the passive block, the power enters the Active Protection Block. The active block is again almost completely unchanged from the LV2b version of this same circuit, and can be seen along with the passive block in the following EAGLE drawing (figure 3). The job of the active protection block is to actively protect the remaining circuitry from damage due to short circuits on either side of the circuit, incoming over-voltages, outgoing over-voltages, over-current, and over-temp conditions. The heart of the active block is Q2250 which acts as a low Rds-on circuit breaker. Q2250 is controlled by U2250 which senses the voltage drop across Q2250 in series with R2252 and R2253. By sensing the voltage drop, U2250 can tell when an over-current has occurred and trip Q2250 off. If the output of the SPS 5V line goes overvoltage, U2251 will cause Q2251 to short to ground. The result is what appears to U2250 to be an over-current, again resulting in tripping of Q2250. This circuit also allows the microprocessor to shut off the SPS power by using Q2282 to short across R2251 resulting in U2250 receiving an off signal on pin 6.

Figure 3: Active Protection Block



The final portion of the SPS is the actual switching power supply itself. This circuit is based on the LT3972, which is a 33V DC input, 1.8V DC to 24V DC output, 3.5Amp, 2.4MHz Buck regulator from Linear technologies. The EAGLE drawing of figure 4 shows the details of the LT3972 circuit. C2201 and C2201 are input filter caps sized to keep switching noise from reaching the remainder of the electronics. C2225 and R2204 provide soft start functionality. C2203 and R2203 provide frequency specific compensation for 1.5MHz. R2202 sets the oscillator free run frequency, and is set to enable the circuit to startup just below the sync frequency of 1.5 MHz coming in on the sync pin. C2204 is placed to help an internal schottky diode on the BD pin to slightly boost the voltage at the boost pin resulting in more efficient operation. R2205 and R2206 setup the voltage divider that completes the feedback loop. D2201, L2201, and C2205 complete the buck topology switching power supply. The catch diode D2201 acts to rectify the output of the LT3972. L2201 and C2205 act in concert to low pass filter the output resulting in a solid low noise DC output from the circuit.

Figure 4: GFE Switching Power Supply Circuit



The SPS in concert with the HAP output regulator meets all of the following SPS requirements:

* + Circuit must be fault tolerant/resistant/robust
  + High Efficiency (prolong Battery life)
  + Low Quiescent Current Draw (prolong battery life)
  + High Frequency Switching (1.5 MHZ) (less audio noise)
  + Frequency Sync to external source (Makes noise filtering easier)
  + OVP (survive over-voltages)
  + UVLO (survive under-voltages)
  + Vin (10V, 14.8V, 20V) (Voltage supplied by APS node)
  + Vout1 (3.0,3.3,3.5) V
  + Vout2 (4.8,5.0,5.2) V
  + Iout1 max (0.030,1,)A (range may require changes in component values)
  + Iout2 max (0.030,1,)A (range may require changes in component values)
  + Low noise
  + Soft start

The goal of the SPS is to condition and deliver the power supplied by the APS in a small, robust, fault tolerant package. This is accomplished using the circuits described above. The output of the SPS circuit can be tapped for use directly, or can be further conditioned by the HAP and/or other node specific hardware.

### 2.2 HAP

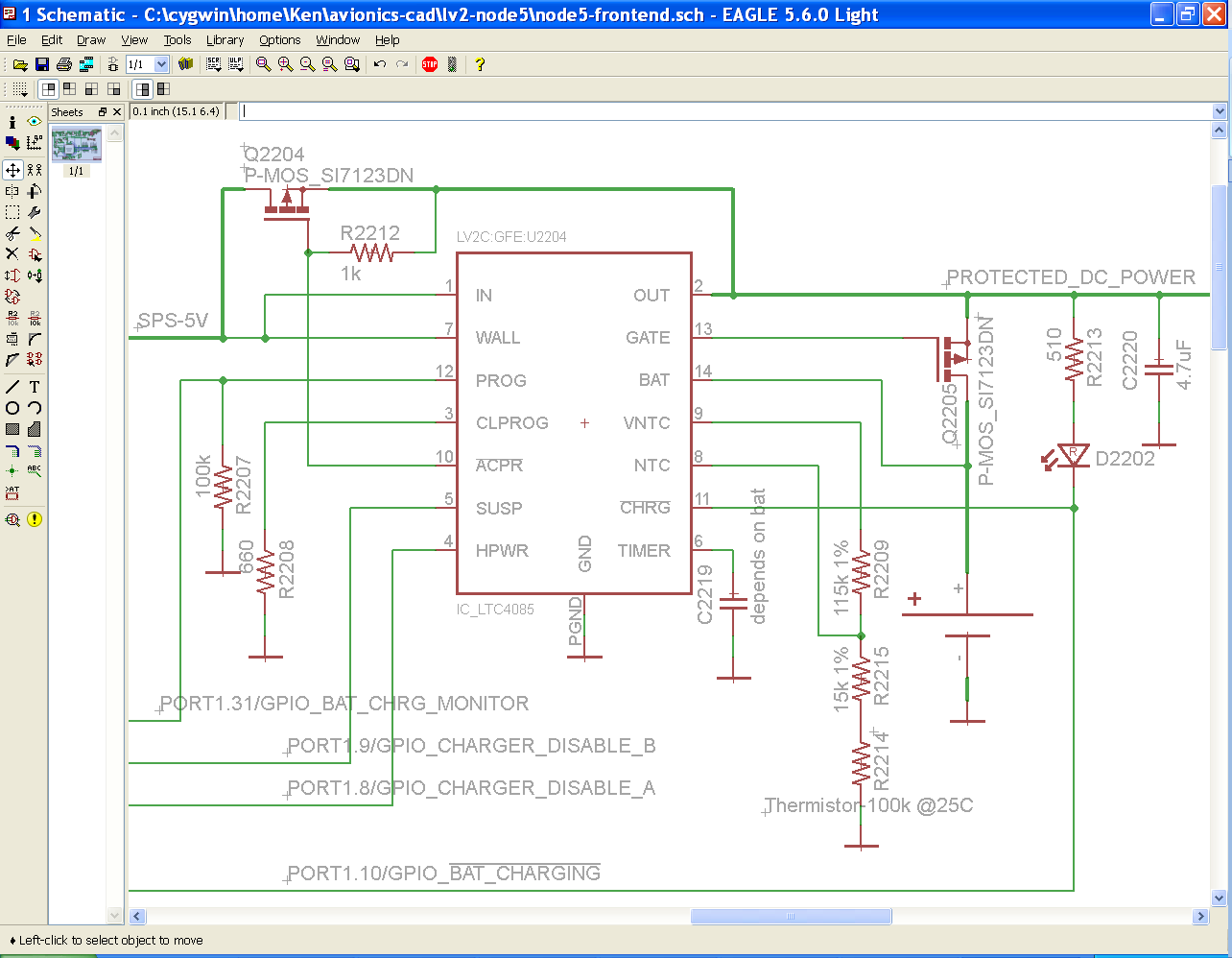
From the SPS power flows next to the HAP, or more specifically to the HAP charger and the HAP bypass switch. The purpose of the HAP is to provide a rock solid power flow to the circuitry on the node. ‘Rock Solid’ in this case means battery backed-up and closely regulated. This is required on some nodes for which a power failure could be disastrous, such as the Pyrotechnic node that is required to deploy the parachute (and eventually the second stage) even in the event of an APS failure. By incorporating this battery backup feature as an option in the generic node, it can be easily implemented during the design of the Pyrotechnic Node or any other node where fault tolerance trumps weight gain. This is an important point in that any extra weight from the battery and its associated charging circuit will result in a lower altitude launch, roughly 0.8 to 1 foot per gram of weight. The HAP consists of three sections: the HAP switch network, the HAP charger and battery, and the HAP output regulator. Each section is monitored and controlled by the microcontroller to ensure proper operation.

There are several possible configurations of the HAP. The first and most obvious choice is where there is no HAP or portion of it populated on the node. This is the case where the SPS is configured to provide 3.3Volts directly to all node circuits and there is no need for 5 volts. The second case is where only the HAP output regulator circuit is populated, and there is no charger or battery. This configuration allows the SPS to feed 5 volts to the HAP output regulator as well as any node circuitry that needs a high current 5 volt line. The HAP output regulator in this case provides the 3.3 volts for the microprocessor and other 3.3 volt circuits. The final case is where the entire HAP is populated, resulting in a battery backed up 3.3 volt rail capable of 1 amp, a low amperage (10-20mA) battery backed up 5 volt rail, and a high amperage (1 amp) 5 volt rail with no battery backup. The following sections will provide more detail for the individual HAP circuits.

The HAP charger and battery actually perform the battery backup functions. The charger circuit only activates to charge the battery when the battery voltage falls below 3.0 volts. The battery is only connected to the load when the load voltage drops below the battery voltage. This is accomplished by seamlessly activating a pair of ideal diodes. One diode is internal to the LTC4085, while the other is external (Q2205) and provides a lower resistance path for the battery current than would the internal diode alone. The HAP switch network is comprised of three Mosfets, two of them are the ideal diodes just mentioned, and the third is Q2204, the bypass switch. During non-battery operation the LTC4085 detects the input power from the SPS and leaves Q2204 near short and connecting the SPS to the HAP output regulator and load. During power failures or other faults causing the disruption of SPS power, loss of power on the in and wall connections will result in the LTC4085 opening Q2204 resulting in a disconnection of the SPS from the load and subsequent connection of the battery as the load voltage drops below the battery voltage.

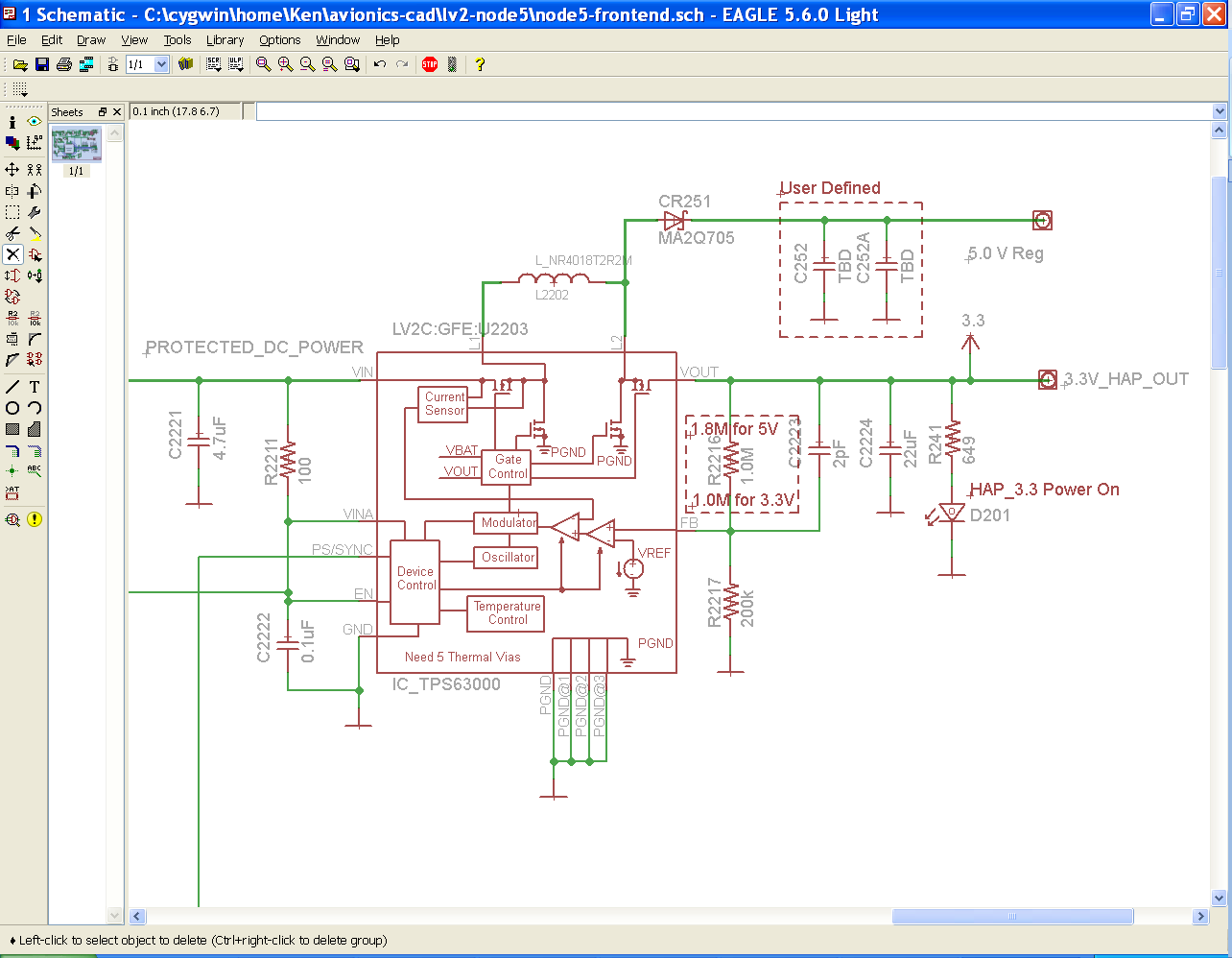
The EAGLE schematic shown in figure 5 shows the HAP charger and switch network in detail. Notice that in this case the battery has not been specified, and as a result the charge timer is not yet set. U2204 is an LTC4085 Li-Ion charger, power manager, and ideal diode controller from Linear Technologies. It serves to charge the battery and control the power path during SPS power failures. As mentioned above, Q2204 is the SPS disconnect switch and allows the SPS to be disconnected from the load. Q2205 is the external ideal diode, controlled by U2204, and activates anytime the Protected DC Power line drops below the battery voltage. This can happen if the SPS is disconnected, or in the unlikely event that the SPS is unable to supply the entire load in which case the battery kicks in the extra current demanded by the load. R2212 acts as a pull-up resistor for the gate of Q2204, allowing it to remain functional when the SPS voltage is missing. R2207 sets the charge current and is monitored by an A/D on the microprocessor, as its instantaneous voltage is directly related to the instantaneous charge current. R2208 is set to limit the amount of current flow that is allowed from the IN pin to the OUT pin, and is set for a maximum of 1.5 Amps, though it is unlikely that much current will flow in that path while Q2204 is populated, and would require that the wall pin be grounded. C2219 is set to determine the length of the charge timer. R2214 is a thermistor used to ensure that the battery is not too hot or too cold for charging. R2215 and R2209 act in concert with the thermistor to set the activation points for the hot and cold trip-points. Q2205 is the above mentioned external ideal diode and provides a low resistance path for the battery current. During charging and normal operation it is open to allow U2204 to monitor and charge the battery. D2202 is a charging LED indicator; R2213 is sized to set the current flow through D2202. The final component is the output capacitor C2220 which serves to ensure smooth transitions to and from battery power.

Figure 5: HAP Charger and Switch Network



The HAP output regulator in the EAGLE schematic shown below (figure 6) is based on the TPS63000 from Texas Instruments. This is an interesting IC designed to provide either 5 or 3.3 volts from a single lithium ion battery, and as such it is well suited to our application. What makes this IC interesting is that during any given cycle, the converter only activates two of its internal switches resulting in operation as either a buck or a boost converter. This is noticeably more efficient than a typical buck-boost converter design. Another advantage of this design is that it is really very simple to implement, with the most important requirement that the output capacitor be large enough to keep the feedback loop from becoming unstable. This can happen with Cout smaller than about 10uF and is not an issue in this circuit implementation. The only nonstandard portion of this implementation is the User Defined section consisting of CR251, C252, and C252A. This portion of the circuit should be able to supply a roughly 5V power line in low capacities that is regulated via the 3.3V supply. As for the remaining components, C2221 is the input noise filter and is in place to shunt switching noise back to the regulator IC. R2211 in combination with C2222 acts to implement a soft start function, and allow Vin to receive power before the device control line at VinA. L2202 is the power inductor responsible in combination with C2224 for output filtering of the final supply rail. R2217 and R2218 are placed to provide a feedback circuit voltage divider, while C2223 is placed to speed up the feedback loop. Current control resistor R241 and LED D201 are in place to provide a visible indication that the 3.3V line is actively powered. In a similar manner to the SPS, the switching speed here is held constant by a 1.5MHz clock signal applied to the sync pin. Applying GND to the EN pin will shut down the regulator, disconnecting the input from the load and leaving all four internal switches in the open position.

Figure 6: HAP Output Regulator



The HAP meets or exceeds all of the following requirements.

* + MUST use single Li Ion Polymer cell
  + MUST have a seamless transition from externally powered to battery-powered
  + MUST meet standard lithium charge/discharge safety requirements (thermal, voltage, current, time, fuse)
  + MUST store enough power to run generic node for (1,4,) hours (Pyro requirement)
  + MUST be able to be unpopulated on board (for most nodes)
  + MUST be able to have external charge control (from microcontroller)

The HAP design does not yet meet the following requirement.

* + MUST be able to measure battery voltage (requires microcontroller A/D pin)

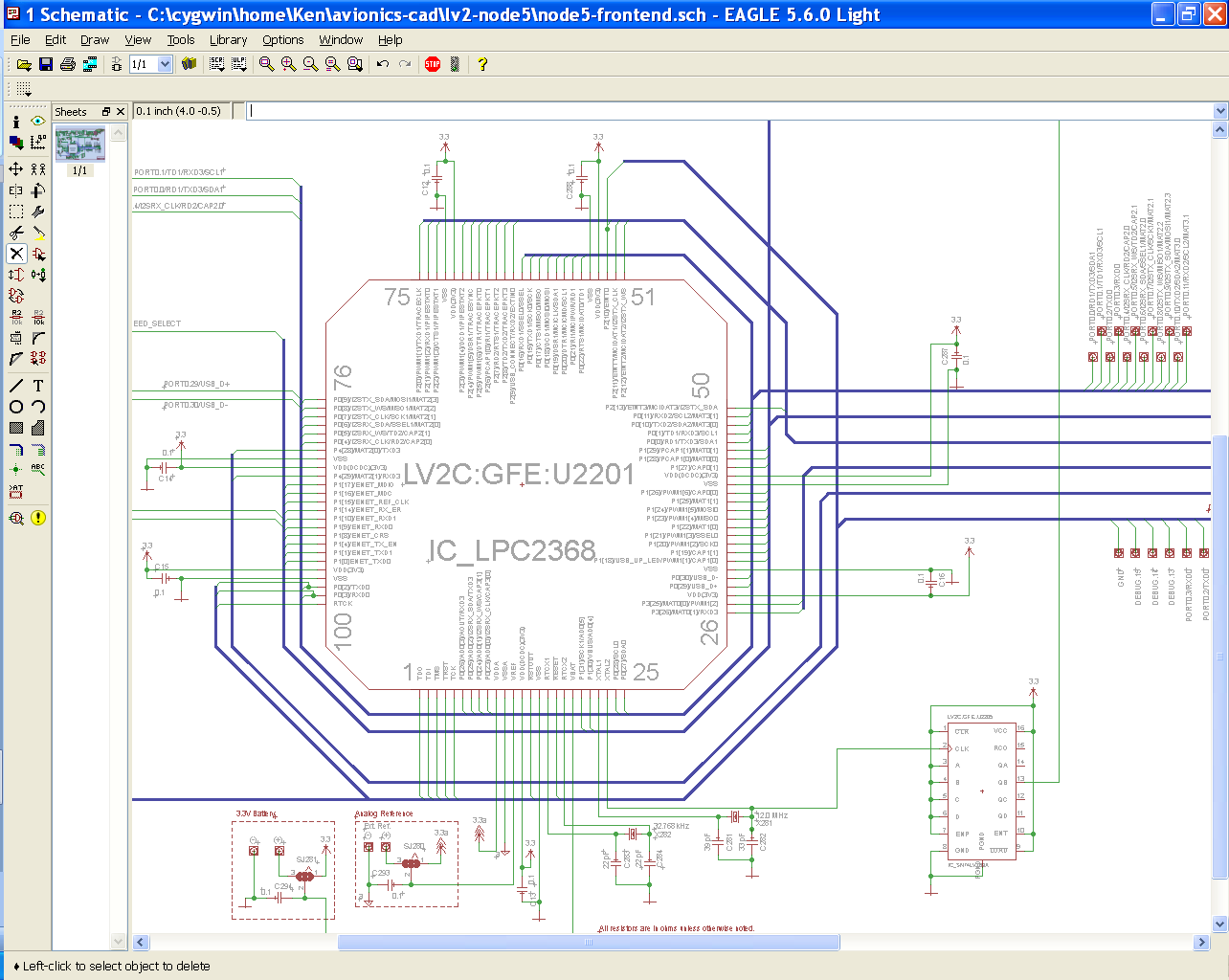
As of this writing the HAP design is not quite complete and there are two glaring problems with the circuit. They should both be addressed before the circuit is implemented. The first is that the EN pin of the TPS63000 (U2203) is currently tied to the input of the device and as such the device cannot be shut down for storage. The second issue is that in order to measure the Battery voltage, another microcontroller A/D line needs to be connected to the HAP circuit at the top of the battery (connect to the BAT line of the LTC4085 (U2202). Aside from these two issues the circuit should perform as required.

### 2.3 Microcontroller and Glue Fabric

The microcontroller chosen for the nodes is the NXP (Philips) LPC2368FBD100. This is a 100pin 32 bit ARM7TDMI-S microcontroller. The LPC2368 is the primary processor for the node, and handles communication with all of the onboard and off-board devices to which it is attached. In the case of the GFE, the LPC2368 connects to external devices via the onboard USB and CAN controllers. There is also a JTAG interface that can be used to setup and checkout the node. The GFE uses 49 of the available pins leaving just over fifty easily configurable interface pins to be used by the node specific hardware. Of the pins in use, many are simple power and ground, though there are also connections in use for GPIO, A to D conversion, USB, CAN, and JTAG interfaces.

The LPC2368 microcontroller comes out of the box with 512kB Flash memory, 58kB of SRAM, GPIO, USB port, SD/MMC port, I2C, I2S, SPI, 2 CAN channels, 6 ADC (10bit), 1DAC (10bit), 3 UARTs, and several PWM controllers onboard the IC. Using the 12MHz external clock as an input to the PLL, the LPC2368 is capable of running at internal frequencies as high as 550MHz, though on power-down, or reset the PLL is disabled and the internal clock is used until the PLL is set by software. In the EAGLE schematic shown in figure 7, the LPC2368 can be seen, along with all the connections to it. In this case, all pins are connected to buses, crystals, or power/ground. Between each of the Power and ground pins there are decoupling capacitors. There are also cuttable jumpers to allow for external connection to analog reference and I/O power pins. At the bottom of the drawing are the two crystals connected to the RTC clock (X2282, 32.768MHz) and PLL input (X2281, 12MHz) pins. The crystals are also connected to ground with a pair of decoupling capacitors each (C2283, C2284, C2281, C2282). In addition to the PLL input pin of U2201 (the LPC2368) the 12MHz crystal (X2281) is used to drive U2205 which is a 4 bit binary counter. The QC output of the counter is then used as a clock signal running at 1.5MHz to sync the SPS and HAP switching DC to DC converters (U2202 and U2203).

Figure 7: LPC2368 Microcontroller



Two of the external interfaces that the LPC2368 microcontroller (U2201) has to the outside world connect through the APS connector and are USB and CAN ports respectively. They can be seen in detail in the following EAGLE schematic (figure 8). As of this writing the CAN circuit is still a work in progress and does not yet have a perfectly functional circuit to implement protection from stuck dominant bits, though it will by the end of the week. U2206 is a 3.3V CAN transceiver and uses R1 to control the maximum slope of the CAN bus signal. U2206 is an SN65HVD235 from TI and can implement a service called Auto-baud. In a nutshell, when Auto-baud is used, the device acts in listen only mode and allows the CAN controller (Internal to U2201) to check for errors while changing baud rates. The baud rate with no errors is the baud rate that the bus is running at. As for the USB ports, they are largely unchanged from LV2b. They start out by using USB Transient Suppressor U2282 to protect them from transient damage. They follow that up with L2281 and L2282 for input filtering, then resistors R2281, R2282 in combination with C2289 and C2290 for further protection of the LPC2368 pins. GPIO from port P1.18 is used to enable USB high speed mode.

Figure 8: USB and CAN Ports

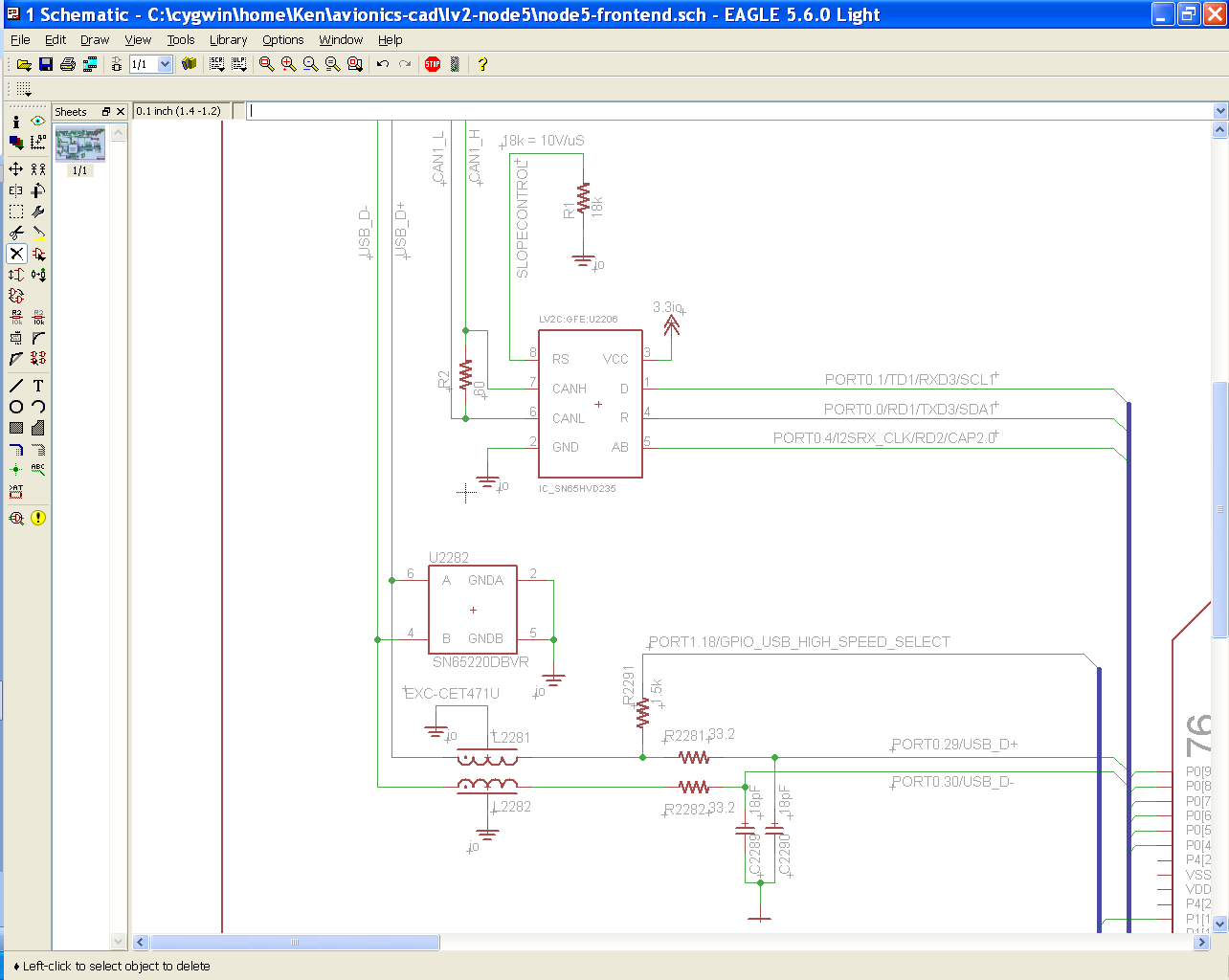
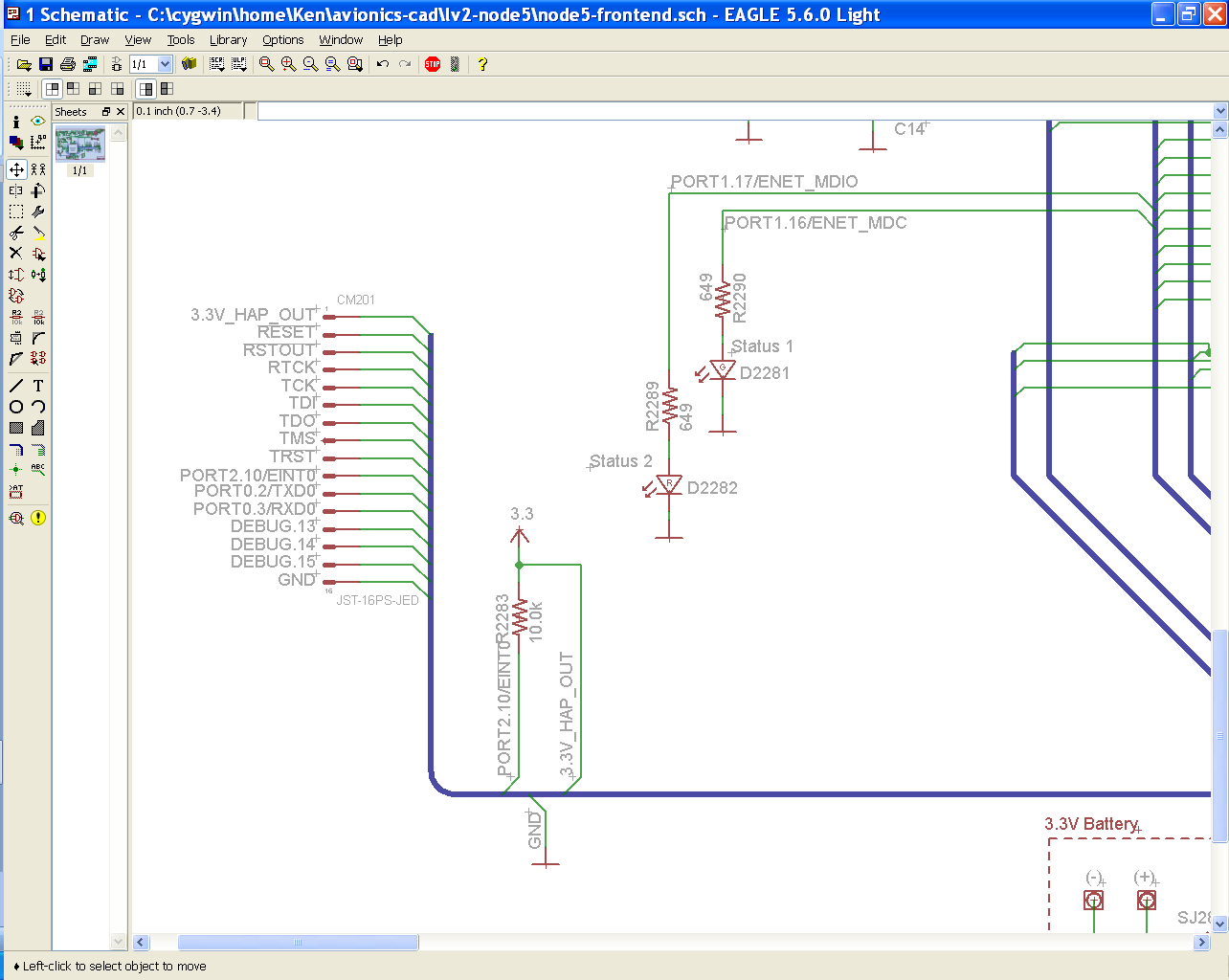


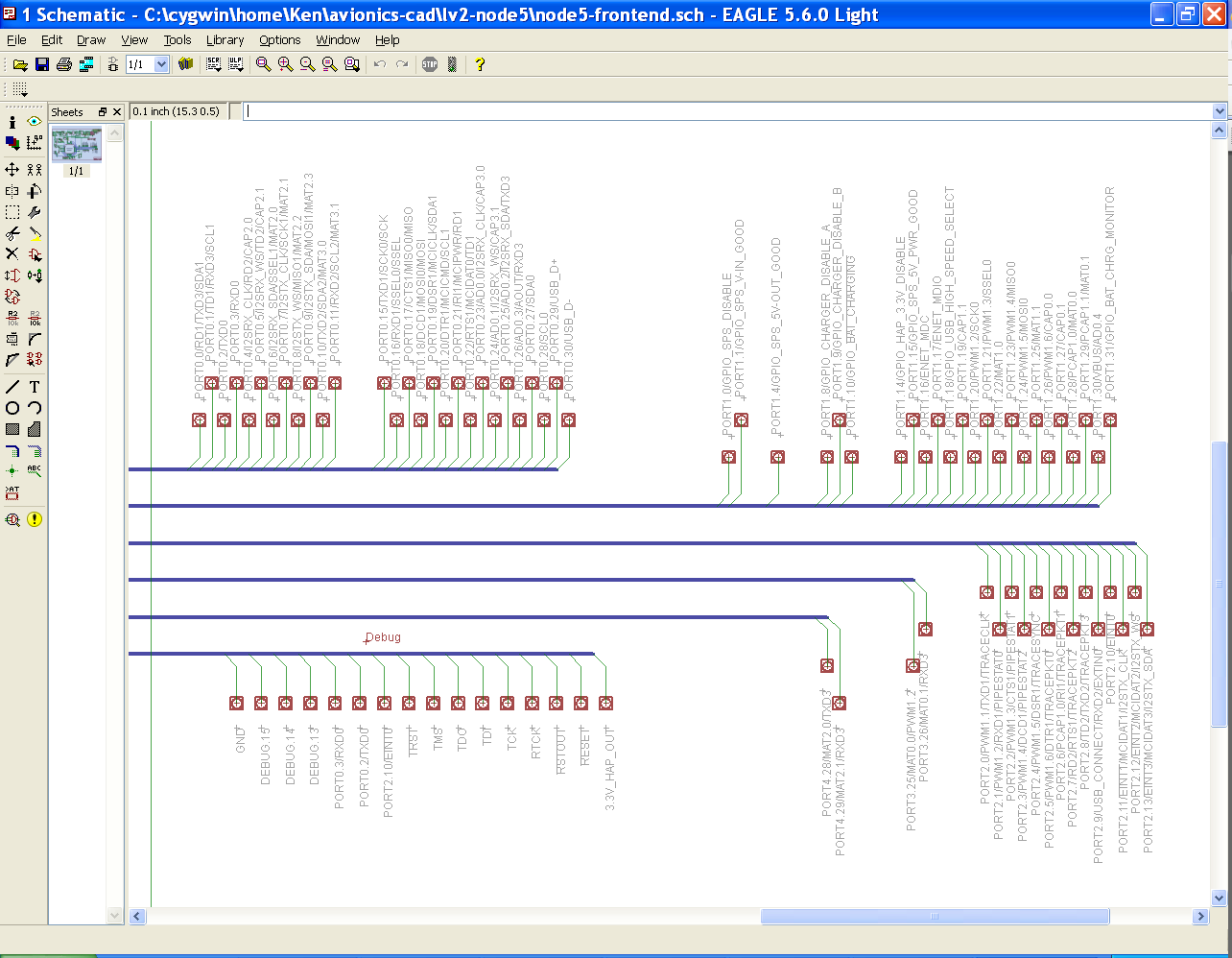
Figure 9 below shows a close-up of the Debug port and the signals on that connector. The JTAG port needs access to UART0, Reset and JTAG signals. Debug signals 13, 14, and 15 are shown for clarity and are not connected at this time. Signals on the debug port include: 3.3V power, !RESET, !RSTOUT, RTCK, TCK, TDI, TDO, TMS, !TRST, !EINT0, TXD0, RXD0, GND. The external interrupt 0 (!EINT0) signal is present for use in resetting the processor and can be seen with its associated pull-up resistor R2283. In addition, this drawing shows the two status LEDs (D2281, D2282) from the original LV2B system along with their associated current set resistors (R2289 and R2290) connected to U2201 on ports P1.16 and P1.17.

Figure 9: Debug Port



Finally, as can be seen in figure 10, all of the available port pins are broken out and named with both port title and signal information. On the layout drawing each of those pins is connected to a small SMD style pad that can be probed, though they are mostly present as placeholders that will allow easy identification and connection of Node Specific Hardware when needed.

Figure 10: LPC2368 Available Port Pins



The microcontroller and glue fabric meet all of the following requirements:

* + MUST use a LPC2xxx series microcontroller
  + MUST have USB and back-channel peripherals
  + MUST have (32,64,) K RAM
  + MUST use 12 MHz crystal (for USB) and PLL to highest Freq.

As the final part of the Generic Front End, the Microcontroller and glue should outperform the LV2B design by a wide margin. There are more GPIO pins available, and the LPC2368 supports the CAN bus in addition to everything the LPC2148 supported. The only real downside is the loss of several channels of A/D converters and the added complications during layout from all of the extra pins. Unfortunately at the time of writing this report, there is still more to do and the design is not yet complete. Some of the remaining work is in the area of the CAN transceiver. It still needs the addition of circuitry to force it to enter Autobaud listen only mode if this node tries to force the CAN bus to a standstill by transmitting an unrelenting Dominant bit. That circuit is on paper, but not yet put together well enough for the final design. In addition, the HAP output regulator needs to have the connection to the microcontroller figured out so that we can be assured of shutting it down when desired. More additional work lies in two further areas. Specifying parts, and completing the circuit layout. Much of the work regarding the layout has been completed, remaining work mostly depends on what node the GFE will be combined with. Many of the signals to and from the LPC2368 remain to be routed, but as Node Specific Hardware could easily require repositioning the microprocessor, it is not a priority to have them routed before the Node Specific Hardware is ready to be routed.

Overall the GFE update went well. There was a phenomenal amount of work to be done as well as steep learning curves for many of the tasks involved. There was a lot to learn about hardware, specifically power supplies, and microcontrollers. In addition to the hardware problems that had to be overcome, there were significant issues ramping up on the different software packages involved. Eagle, GIT, and the wiki were all completely new to the team and they all took time to learn, even with the fantastic amounts of help from the PSAS sponsors.

# 3 Avionics Power System (APS) Overview

The Avionics Power System serves several important functions for the LV2c rocket. First, this node distributes main battery/shore power to the other avionics nodes via a network of power switches which also provide overcurrent protection, distribute data signals, and a means by which the microcontroller can control which of the attached devices actually receive power.

Second, the APS employs an umbilical connection to ground based computer systems which simultaneously charges the APS main battery and powers the rocket during charge. The umbilical connection also provides a means by which the ground computer can directly communicate with the APS microcontroller.

The APS also contains a USB (Universal Serial Bus) Hub integrated circuit which distributes USB communication signals from the main flight computer to other avionics nodes via the power switch connectors.

Finally, a network of sensors provides real time information as to the status of the rocket’s main battery. This includes LED indication of battery charge, current and voltage measurement, and various other sensors.

The design and implementation of each of the components described above, along with battery selection, are described next.

### 3.1 APS Power Switches

Each of the APS power switches combines a controller IC with an external MOSFET to control the distribution of main battery power, as well as various data signals, to the other avionics nodes via 16 pin, locking connectors. Each switch provides a means of overcurrent and undervoltage protection to the attached device, as well as a means by which the microcontroller can control which of the attached devices receives power.

There are several reasons for the redesign of this portion of the APS. First, the previous version only supported power switching for attached devices. A key difference between the LV2b and LV2c is that the latter aims to provide a wider range of adaptability and versatility by designing its systems not only with the most current technology, but with the ability to upgrade and add new technologies as they become available. As such, the LV2c has been designed with a power switch network capable of supporting up to 7 peripheral devices, as well as an upstream flight computer. Designed in this way, nodes can be added or removed from the rocket as design updates may require. Further, the LV2c uses several different forms of data for communication between nodes and the flight computer. As such, a new design was required to allow this change.

Another reason that the switches required redesign is due to the fact that the switch network of the LV2b was implemented using ICs whose maximum operating voltage was near the level at which the APS normally functions. Due to this fact, the old network was very susceptible to issues regarding surges and transients.

Finally, the previous power switches were relatively complicated circuits and, as several years had passed since the design of the LV2b APS, it seemed reasonable that newer technology had been developed that would allow simpler designs. Figure 11 on the following page shows a schematic of one of the power switches from the LV2b APS. Figure 12 then follows depicting a schematic of one of the 7 power switches designed for this project.

Figure 11: LV2b Power Switch

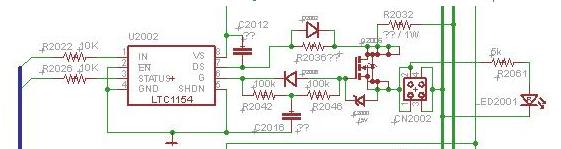
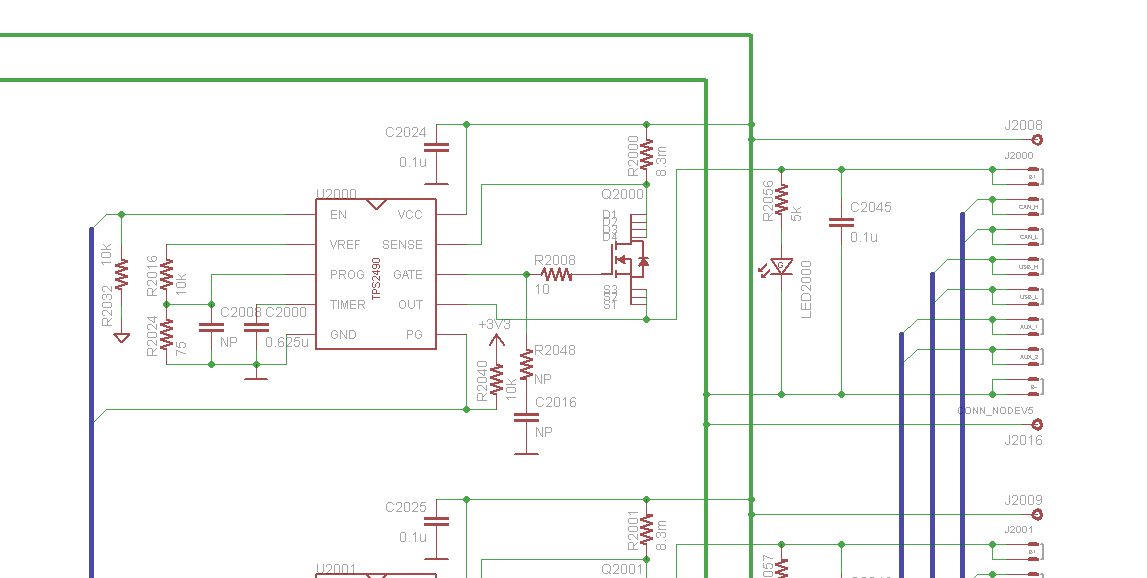


Figure 12: LV2c Power Switch

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As comparison of the above circuits shows, the LV2b and LV2c switches each require a similar number of external components, however the LV2c design only requires resistors and capacitors, where the previous design required the use of several diodes.

#### 3.1.1 Power Switch Circuit Design:

The design of the APS power switches was essentially a matter of choosing the appropriate controller IC and external N-Channel MOSFET. The 16-pin connector which provides the physical interface between the APS and connected nodes also had to be designed. Since the battery voltage is approximately 14.8V with a 8.5A current, we required devices with reasonably wide operating ranges. The switches were also required to meet the following requirements given by PSAS:

*APS Power Switch Design Requirements:*

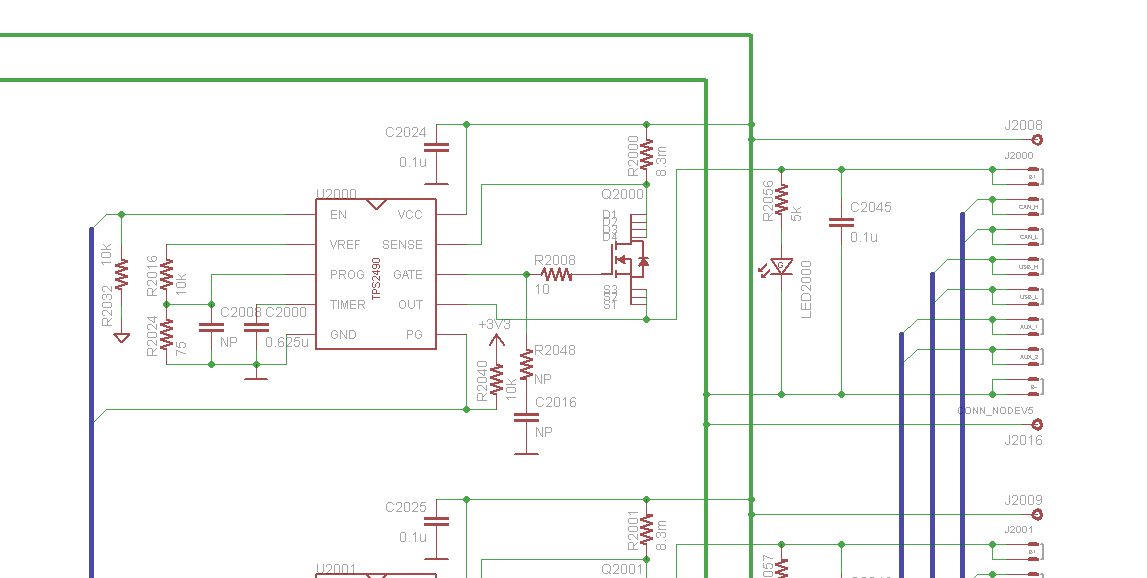
* + MUST have (8,,) independent resettable electronic circuit breakers with adjustable current trip and trip delay. Setting can be via resistor strap, EEPROM, etc. Current trip should be latch-off or selectable.
  + MUST have Soft on/off feature
  + MUST have no mechanical switches in main power path.
  + MUST indicate power switch on/off state (LED for human, and electrical signal for APS node)
  + MAY indicate power switch fault state
  + MUST operate continuously within 20% of the over-current set point
  + MUST allow set currents in the range (0.1, 5)A
  + MUST allow over current transients of 100% for minimum 100 ms without fault to the load

Along with these requirements, and the knowledge of the operating conditions of the APS, thermal considerations needed to be made in the interest of ensuring that the external FET would not overheat and fail. All of these things in mind, research led to the TPS2490 Hotswap Controller IC and Si4122DY N-Channel MOSFET. Both devices are rated to easily handle the operating voltages and currents of the APS; the TPS2490 has an operating range between 9-80V and the Si4122DY has a maximum Vds of 40V with an R\_dson of 4.5 mA. As will be discussed, these devices also function well to meet the above requirements.

The TPS2490 acts as a current controlled circuit breaker, meaning that it turns on the external FET when the current is within some set range, and turns off the FET and breaks the circuit when that range is exceeded by some specified amount for some period of time. A close-up view of the switch in figure 12 is shown below in figure 13 to aid in the functional description. To better explain the circuits functioning, below is a detailed pin description of the TPS2490, followed by a more in depth description of the IC’s functionality. Appendix B, at the end of this report provides detailed descriptions of each of the circuit components used in the actual design.

Before detailing the integrated circuits used, the connector to which the power switches provide an output, and peripheral devices connect to had to be redesigned to support CAN and USB signals as well as provide power. For this component, a 16 pin JED connector was used. For the purpose of reliability of the system, it was required that these connectors contain a locking mechanism similar to that of a monitor connection of desk top PC’s in which the male end of the connector essentially screws into the female. These 16 pin connectors were modified to employ similar screw holes for APS nodes. The schematic symbol of this component can be seen in the far right of figure 12.

Figure 13: LV2c Power Switch Circuit Close-up

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#### 3.1.2 TPS2490 Pin Descriptions

**VCC:**

This pin serves 3 functions (See Function Descriptions for explanations of specific functions):

1. biasing power to the controller IC
2. Input to power on reset (POR) and under voltage lockout functions (UVLO)
3. Voltage sense at one of the terminals of sense resistor Rs (See Typical Application diagram on page 1 of datasheet)

**SENSE:**

This pin connects to the downstream terminal of sense resistor (R2000 in figure 13). This pin monitors the voltage at the FET drain and R2000 terminal to provide feedback to the controller's constant power limiting engine (see Function Descriptions) as to FET current (Id) and voltage (Vds). Id is calculated using voltage difference between VCC and SENSE pins divided by the value of sense resistor R2000. Vds is calculated with the difference between voltages on SENSE and OUT pins.

**GATE:**

This pin provides the high side gate drive for the FET. This pin is controlled by the internal gate drive amplifier which provides a pull-up of 22uA from an internal charge pump and a strong pulldown to ground of 75mA. Pull-down current is a non-linear function of the amplifier overdrive providing small overdrive for small overloads, and large overdrive for fast reaction to output shorts. This pin also employs a separate 2mA pull-down to shut off the transistor when the voltage on EN pin, or UVLO (see functional descriptions) conditions cause this to happen.

**OUT:**

This pin is used by the constant power engine and PG comparator to measure Vds of the transistor. Internal protection circuits leak a small current from this pin when it is low.

**EN:**

The TPS2490 gate drive is enabled if the positive threshold is exceeded and internal POR and UVLO thresholds have been satisfied. If the IC is latched off, it can be reset by cycling the EN pin below the negative threshold and then back high. The voltage thresholds for this pin are as follows:

* V-EN-High: typical 1.35V
* V-EN-Low: typical 1.25V

**VREF:**

This pin provides a 4V reference voltage for use in setting the voltage on the PROG pin. This voltage is available once the UVLO threshold of 8.3V has been satisfied. This pin supplies no more than 1mA of current.

**PROG:**

The voltage applied to this pin programs the power limit used by the constant power engine. The voltage on this pin is set using a resistor divider circuit on the VREF pin.

**TIMER:**

An integrating capacitor, C2000 in fig13, connected to this pin provides a timing function that controls the fault time. The TIMER pin charges the capacitor with a 25uA current whenever the TPS2490 is in power limit or current limit, and discharges at 2.5uA otherwise. If the voltage on the TIMER pin reaches 4V, the controller pulls the gate to ground, latches off, and discharges capacitor Ct.

**PG:**

This open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PG pin goes open drain (high-voltage with pull-up) after Vds of FET M1 has fallen to about 1.25V and a 9ms deglitch time has passed. PG is false (low) when EN is false, Vds is above 2.5V, or UVLO is active.

**GND:**

This pin is connected to system ground.

#### 3.1.3 TPS2490 Functional Description

The TPS2490 functions by measuring the voltage across R2000 and comparing that value to an internally set threshold of 50mV. If this threshold is exceeded by an overcurrent condition, the TIMER pin outputs a 25mA current which then charges C2000. If when C2000 reaches 4V, the overcurrent condition is still present, the GATE pin is pulled low with a strong pulldown and the FET is turned off. With this functionality, it is clear that the actual current limit for the switch can be set by the value of R2000. Similarly, the duration of time that an overcurrent condition is allowed before turning off the FET is determined by the value of C2000. The two other key functions of these switches are Under Voltage Lockout (UVLO), and the “Power Limiting Engine.” The IC also has the option of a soft-start function, and dV/dt control of the rate at which the gate of the FET is charged. Each of these functions is described next.

**3.1.3.1 Under Voltage Lockout (UVLO)**

This function will disable the switches in the event of a hard short on the main power path. The switches will latch off if the voltage on VCC reaches or falls below 8.3V.

**3.1.3.2 Constant Power Engine**

This function monitors the power dissipation in the external MOSFET for the main purpose of limiting rise in the junction temperature of the FET. The thermal ratings of the FET are used to determine the value of maximum power dissipation allowable without damage to the device. From the datasheet description, this function generally applies to startup conditions as this is when the FET will experience inrush over-currents and run the risk of exceeding its physical limitations. This, in turn, can result in not only damage or destruction of the FET, but damage or destruction of the attached device as well. The constant power engine varies the transistor current, Id, as the voltage, Vds, changes in order to ensure that power dissipation remains constant at the programmed value. As stated, the actual power limit value is determined using thermal parameters of the FET used in the design in the following equation:

Where:

* Rthjc = FET junction to case thermal resistance (42 degC/W)
* Tjmax2 = short term max die temp. of FET, can be set at 150C if max rating is 175C, since Si4122DY max is 150C, we'll set this to 150C - 25C = 125C
* Rdson is the FET on resistance at max operating temp. of about 80C. This value is 4.5mOhm
* 0.7 represents the tolerance of the constant power engine
* Rthca = the max case to ambient thermal resistance; equal to Rthja - Rthjc = 21degC/W
* max = the square of the max drain current, Id, allowed (5A) = 25
* Tamax = maximum ambient temperature (assuming around 70C)

Using the above equation Plim can be calculated

Plim <= 1.755W

This value can then be programmed into the TPS2490 by applying the voltage to PROG pin which satisfies the following equation given in the datasheet:

VPROG = Plim/(10xIlim)

This equation is derived from the fact that the constant power engine has an output clamped to 50mV according to:

Solving for VPROG:

Since Plim = Ilim x Vds = Ilim x (VSENSE - VOUT):

The calculated VPROG is applied to the PROG pin using a resistor divider circuit in conjunction with VREF. See component selection in appendix B for resistor values and calculations.

At startup we can assume that Vds = VCC. The initial current through the FET, Id-allowed, is then determined by the set power limit according to:

After stepping to this initial value of Id-allowed, Vds falls and Id is allowed to increase in such a way as to ensure that Plim remains constant. This happens because the power limiting engine adjusts the current limit reference to the gate amplifier thus controlling the transition of the FET from off to fully on, and allowing the transients to pass before it reaches the fully-on state. In non-startup overcurrent conditions, power limiting is assumed to be achieved in a similar fashion. In this situation the voltage at VSENSE will increase due to the rise in current through sense resistor R2000 and Id-allowed will be adjusted to ensure that the power dissipation remains constant according to the set limit.

**3.1.3.3 Soft-Start**

In the description of the constant power limiting engine, it is mentioned that at startup there is a small step-up in Id-allowed to satisfy the power limiting engine. This initial step up in current could pose a potential problem depending on its magnitude. As such, the switch can be designed with a capacitor added to the PROG pin to employ a soft-start function which converts this step into a ramp. The value of the capacitor would then determine the slope of the ramp. See C2008-C2015 in appendix B for more information about the circuit components used.

**3.1.3.4 dV/dt Control**

The TPS2490 provides the option of dV/dt control in applications which require constant turn on currents for the FET. This is achieved through the addition of a resistor in series with a capacitor connected from the GATE pin to ground. See C2016-C2023 and R2048-R2055 in appendix B for component information.

#### 3.1.4 Power Switch Design Verification

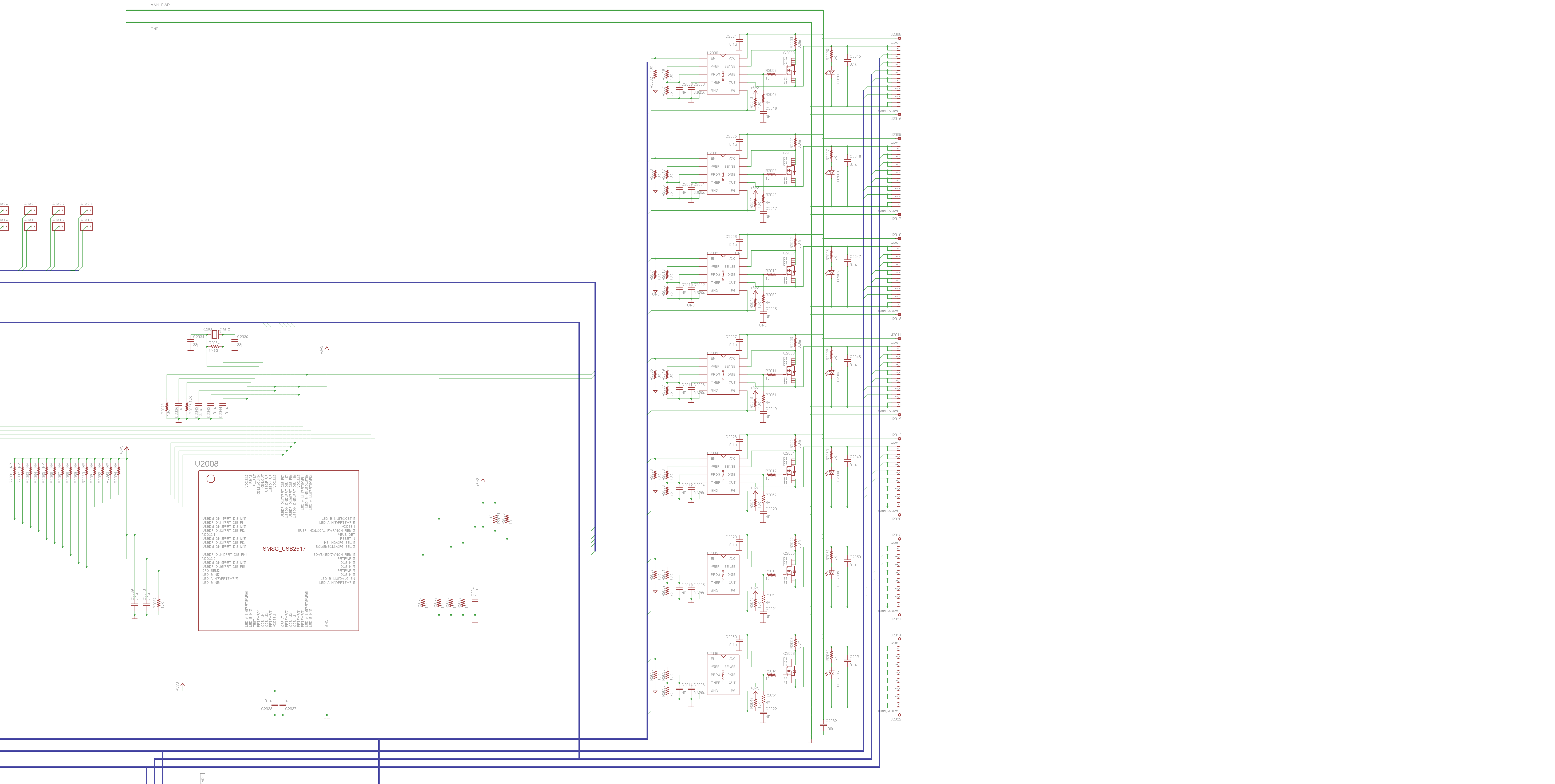
With the above functional descriptions, we now revisit the design requirements to verify that they have indeed been met.

*APS Power Switch Design Verification:*

* + Design includes 8 independent resettable electronic circuit breakers with adjustable current trip and trip delay. Setting via resistor strap. Current trip latch-off.
  + Design provides option of soft-start
  + No mechanical switches in main power path.
  + Indicates power switch on/off state (LED for human, and Power Good signal for APS node)
  + Designed to operate continuously within 20% of the over-current set point (See R2000-R2007 in Appendix B)
  + Allows set currents in the range (0.1, 5)A
  + Allows over current transients of 100% for minimum 100 ms without fault to the load (See C2000 – C2007 in Appendix B)

Based on this verification it can be concluded that this is an adequate design of the APS power switches in that each of the requirements has been met. Figure 14 on the following page shows a bird’s eye view of the EAGLE schematic for the 7 power switches.

Figure 14: APS Power Switches

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### 3.2 APS Umbilical Connection

The umbilical connection for the APS provides a means for the ground based flight computers to communicate with the rocket prior to a launch, while also providing shore power to charge the APS main battery and power the rocket during battery charging. The requirements given for this portion of the APS are shown below.

*APS Umbilical Connection Requirements*

* MUST seamlessly shift between shore power and battery power
* MUST be able to detect the presence of shore power
* MUST wake up APS microcontroller if shore power turned on
* MUST be able to sense if connector is inserted or removed (launch detect)

Before beginning the design process for this portion of the APS, we were given that the umbilical connector itself had been chosen by PSAS to be a 5 pin connector which provides the following signals: shore power, shore ground, rocket ready, shore transmit and shore receive. These were the signals around which the umbilical interface would be designed.

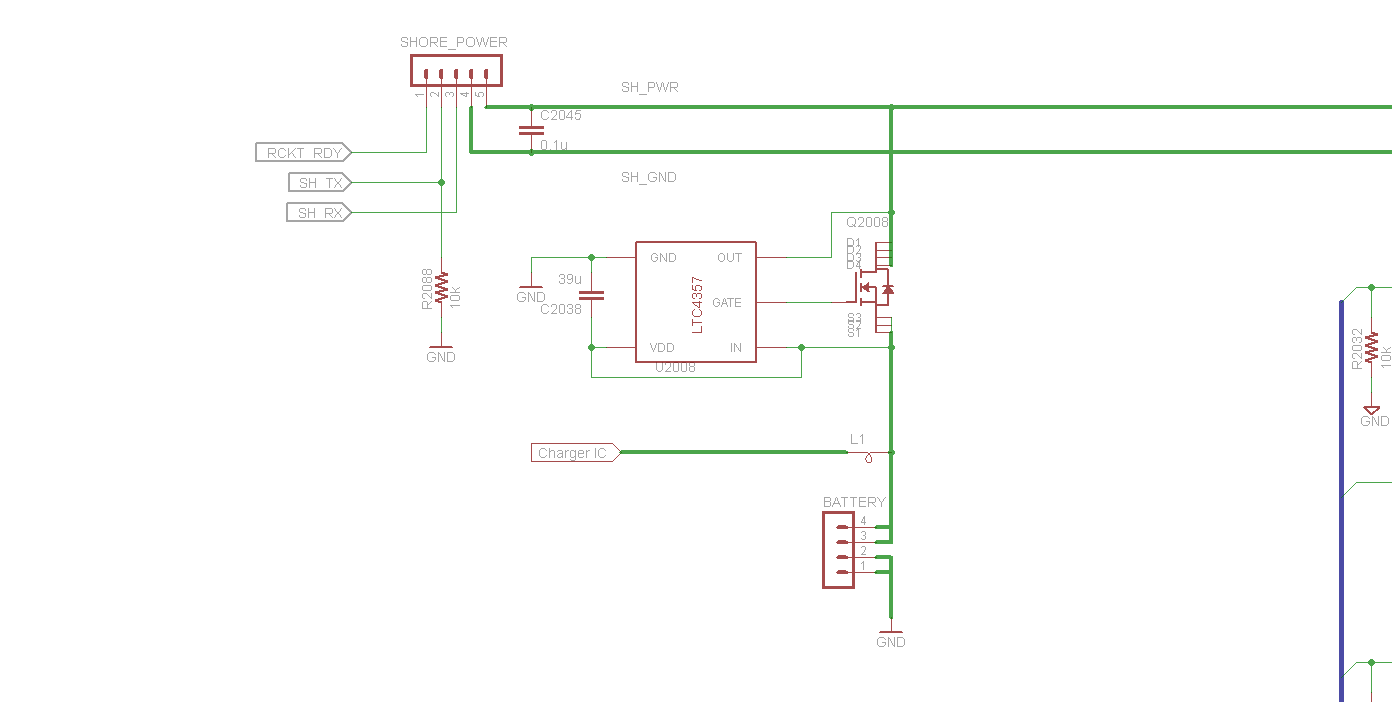
#### 3.2.1 Circuit Design

Refer to Appendix C for detailed description of parts used in this circuit. The requirement for a seamless shift between shore power and rocket battery power was initially implemented using an ideal diode to control which power source was actually supplying the rocket. This design was later discarded, as it was decided that the rocket would utilize an external battery charging system rather than an on-board circuit to handle charging. However, since the Capstone Team did complete the preliminary design for the umbilical, including the ideal diode, these circuit components are discussed here. Figure 15 on the following page shows a schematic of this circuit.

As can be seen in the figure, the ideal diode is simply a MOSFET with a controller IC. The IC's IN pin connects to the source of the FET. The source then becomes the anode of the ideal diode. The OUT pin connects to the FET's drain which acts as the ideal diode's cathode. The LTC4357, which is the ideal diode chosen for this circuit then detects the voltages at each pin and the GATE pin drives the gate of the FET to maintain the forward drop at 25mV. If the voltage across IN to OUT becomes more negative than -25mV, the gate of the FET is pulled low with a strong pull down. This would occur in the event that shore power is present.

Another aspect of this circuit’s design was the launch detect signal. The purpose of this signal, as the name implies, is to signal the APS microcontroller that launch has occurred. This has been designed to occur in the event that the umbilical connection has been unplugged. In other words, when the rocket leaves the launch pad, the umbilical is pulled out of its connector. The resistor R2088, then pulls the shore transmit signal low, which is sensed by the microcontroller. This then indicates to the processor that launch has in fact occurred.

Figure 15: APS Umbilical Interface Circuit

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### 3.3 APS USB Hub

The previous version of the APS employed on the LV2b rocket did not include a USB hub. However, since the new design of the APS distributes data signals, as well as battery power to the attached devices, it was decided that an onboard hub would be beneficial to the LV2c APS design.

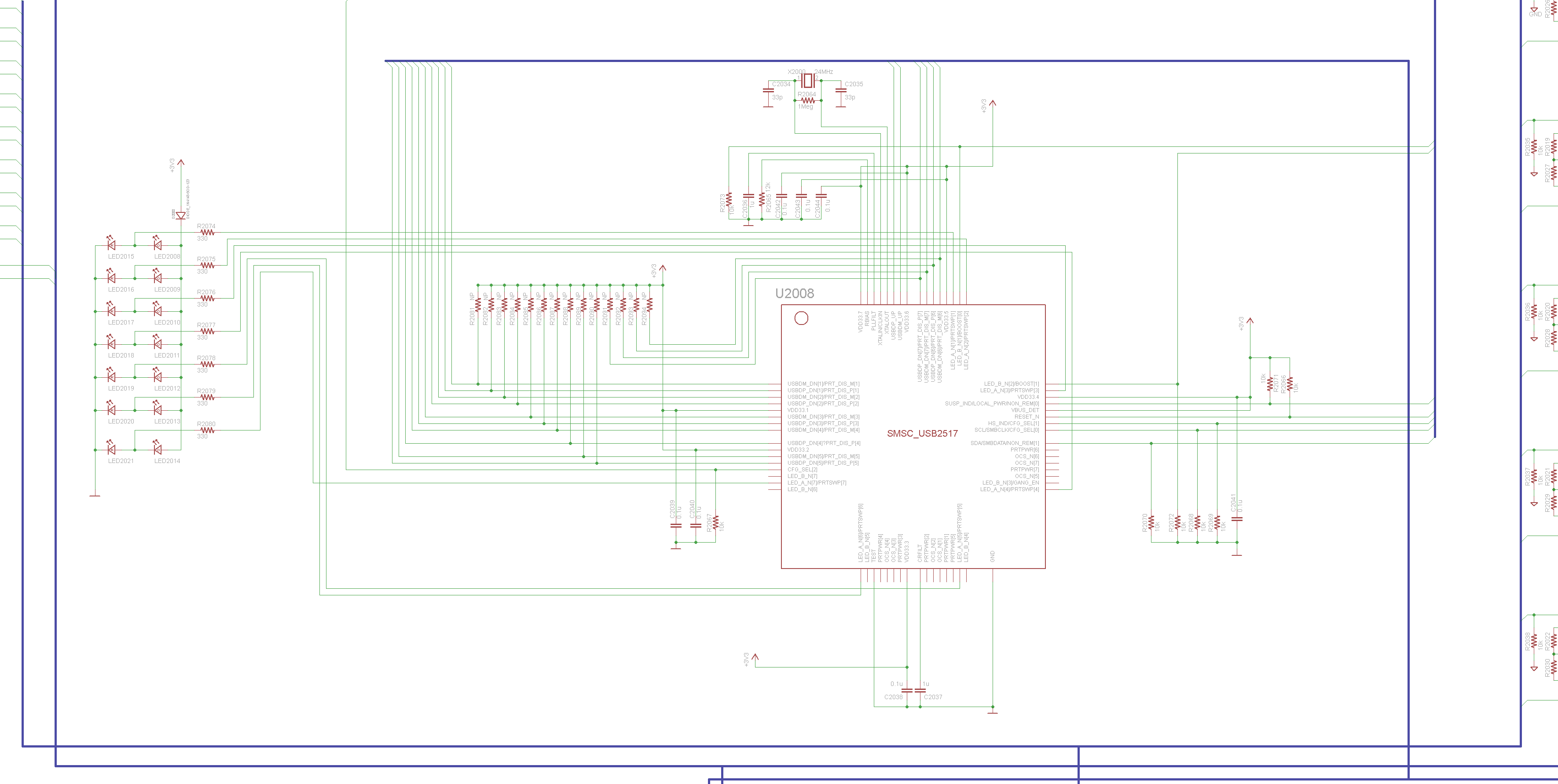
The IC chosen for the HUB is the SMSC-USB2517 due to the fact that it effectively performs the tasks of USB data distribution, and also has many configuration options to ensure that future updates to the APS design could be supported. The requirements for the US B Hub were as follows.

*APS USB Hub Requirements*

* SHOULD be USB 2.0 compliant High Speed (480 Mbps)
* MUST handle (8,,) downstream devices (devices may be further hubs)
* SHOULD have hub status LEDs

Figure 16 below shows the EAGLE symbol created for the SMSC-USB2517.

Figure 16: USB2517 EAGLE Symbol

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As the figure shows, the SMSC-USB2517 hub controller comes in a 64 pin package. It is an OEM (Original Equipment Manufacturer) configurable integrated circuit which uses a multi-transaction translator (MTT) and is capable of supporting 7 downstream ports. The hub supports low, full and high speed devices on all of the enabled ports. All required resistors on the downstream ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-up and pull-down resistors on D+ and D- pins. The over-current sense pins for the downstream ports have internal pull-up resistors as well.

Some key features of the USB2517 include:

* low power dissipation, high performance, small footprint
* Fully compliant with USB 2.0 specification
* 3 options for hub configurations: I2C (via EEPROM), SMBus, and internal default configurations via strapping options

The USB2517 also offers a PortMap flexible port mapping ability, PortSwap which allows programming of USB differential pair pin locations, and PhyBoost which provides programmable USB signal drive strength. Following is a detailed list of pin descriptions which also describes how each pin is connected on the APS. For a detailed description of each of the circuit components used in the Hub design, see Appendix D at the end of this report.

#### 3.3.1 SMSC-USB2517 Pin Descriptions and Circuit Design

**USBDM-DN[7:1]/PRT-DIS-M[7:1]**

* These pins provide one of the two differential USB data signals to downstream ports 1-7
* each of these pins is connected to the pair of the USB\_L pins of the respective power switch port connector
* Pulling any of these pins, along with the associated USBDP pin, up to 3.3V with a 10kOhm resistor disables the respective port
* Instead of pull-up to 3.3V, we will connect these pins to the ARM giving it control of what ports are enabled

**USBDP-DN[7:1]/PRT-DIS-M[7:1]**

* This pins proved the other of the two differential USB data signals to downstream ports 1-7
* Each of these pins is connected to the pair of USB\_H pins of the respective power switch port connector
* Pulling any of these pins, along with the associated USBDM pin, up to 3.3V with a 10kOhm resistor disables the respective port
* Instead of pull-up to 3.3V, we will connect these pins to the ARM giving it control of what ports are enabled

**VDD33**

* There are a total of 7 of these pins, each connected to +3.3V

**LED-A-N[7:1]/PRTSWP[7:1]**

* These pins connect to LEDs which are used to indicate both connection status and port speed for each of the 7 ports.
* This is done with a combination of a red and a green LED assigned to each port.
* See section 6.1.2 on page 29 of the USB2517 datasheet for more information
* Also see LEDs in the component selection
* These pins also are used to configure the portswapping option, which we are not using. To ensure port polarity swapping does not inadvertently occur, these pins must be low when RESET\_N is asserted.

**LED-B-N[7:3]**

* These pins connect to amber LEDs which indicate overcurrent conditions on downstream ports
* We are not using overcurrent sensing so these pins are not connected

**LED-B-N[2:1]/BOOST[1:0]**

* These multifunction pins can connect to amber LEDs which indicate overcurrent conditions on downstream ports
* They are also sampled after RESET\_N is asserted to determine the signal strength of the USB differential signals to downstream ports as follows:
  + BOOST[1:0] = '00': Normal signal strength
  + BOOST[1:0] = '01': approximate 4% signal boost
  + BOOST[1:0] = '10': approximate 8% signal boost
  + BOOST[1:0] = '11': approximate 12% signal boost
* In my current design, the signal strength is set at normal strength so these pins are strapped to ground. However these pins could be connected to the ARM so that signal strength can be controlled on-line

**OCS\_N[7:1]**

* Overcurrent sense input pins. We are not using overcurrent sensing function of hub. Since these pins are pulled up internally, they are treated as no connects.

**PRTPWR[7:1]**

* These pins provide power to downstream ports.
* We are using a separate power switch network so this pins are treated as no-connects

**TEST**

* Used by the manufacturer for IC testing. Must be connected to ground

**CRFILT**

* VDD core regulator filter capacitor.
* Datasheet states this pin must be connected to ground through a 0.1uF capacitor

**RESET\_N**

* This active low pin resets the USB2517 after it is asserted for 1us
* After this pin is asserted, the configuration pins are sampled to determine how the hub is configured
* This pin is pulled up to 3.3V with a 10kOhm resistor and will also connect to the ARM so that configuration can be done on-line

**VBUS\_DET**

* Detects upstream VBUS power
* The datasheet states that in self powered applications, which ours is, this pin must be tied to 3.3V

**SUSP-IND/LOCAL-PWR/NON-REM[0]**

* SUSP-IND:
  + As I understand the datasheet, this function of the pin supports an LED which indicates whether the USB is configured.
  + If asserted, the hub is configured and USB is active
  + If negated, hub is unconfigured or configured and in USB suspend
  + The active state of the LED is determined by the values of NON-REM[0] and NON-REM[1] (see below)
* LOCAL-PWR:
  + Detects availability of local power source
  + Low = Self/local power source is NOT available (Hub is powered only with VBUS power)
  + High = Self/local power source is available
* NON-REM[0]
  + This is a configuration strap option
  + For this function, this pin along with NON-REM[1] is sampled at assertion of RESET-N to determine which, if any, of the downstream devices are removable
  + Which ports are removable is determined as follows using NON-REM[0] and NON-REM[1]:
    - NON-REM[1:0] = '00': All ports removable, Suspend indicator LED active high
    - NON-REM[1:0] = '01': Port 1 is non-removable, Suspend indicator LED active low
    - NON-REM[1:0] = '10': Ports 1 and 2 are non-removable and LED is active high
    - NON-REM[1:0] = '11': Ports 1, 2 and 3 are non-removable and LED active low
* LOCAL-PWR and NON-REM[0] seem to be contradictory for our purposes. At this point I have this pin permanently tied to ground along with NON-REM[1] so that the hub is permanently configured for removable devices on all ports. However doing this would then tell the hub that self/local power is NOT available. My thought is that this pin will need a weak pull-up and also be connected to the ARM which can drive the pin low at assertion of RESET-N. This way, the hub will be configured with all removable devices and still detect local power, which is all we are using.

**SDA/SMBDATA/NON-REM[1]**

* Another multifunction pin used for hub configuration
* SDA
  + Serial data signal
* SMBDATA
  + Server message block data signal
* NON-REM[1]
  + Used in conjunction with NON-REM[0] to determine which, if any devices attached to the downstream ports are removable. See NON-REM[0] description for explanation

**SCL/SMBCLK/CFG\_SEL[0]**

* A multifunction pin used in hub configuration
* SCL
  + Serial clock signal
* SMBCLK
  + System management bus clock signal
* CFG-SEL[0]
  + Sampled at RESET-N assertion in conjunction with CFG-SEL[1] and CFG-SEL[2] to determine which internal default configuration of the hub is used. See CFG-SEL[2] description for further explanation of these options.
* I am assuming that we are not using a serial clock signal or system management bus clock so these signals are not used in the hub circuit at this time

**HS-IND/CFG-SEL[1]**

* Another multifunction pin used in hub configuration
* HS-IND:
  + The pin can support an LED which indicates whether the hub is connected at high speed
  + Asserted = hub connected at high speed
  + Negated = hub is connected at full speed
* CFG-SEL[1]
  + Sampled at RESET-N assertion in conjunction with CFG-SEL[0] and CFG-SEL[2] to determine which internal default configuration of the hub is used. See CFG-SEL[2] description for further explanation of these options
  + If CFG-SEL[1] = '0': HS-IND is active high
  + If CFG-SEL[1] = '1': HS-IND is active low

**CFG-SEL[2]**

* Sampled at RESET-N assertion in conjunction with CFG-SEL[0] and CFG-SEL[1] to determine which internal default configuration of the hub is used.
* See table 8.2 on pages 33 and 34 of USB2517 datasheet for the different default configuration options which can be set using CFG-SEL[2:0]
* For our design CFG-SEL[2:0] = '000' which means the following:
  + Strap options enabled
  + Self-power option enabled
  + LED mode = speed
  + Individual power switching
  + individual over-current sensing

**USBDP-UP**

* One of 2 signals of the differential USB data signal from an upstream device
* This pin is connected to the USB-H pins on the connector to the flight computer (J2007)

**USBDM-UP**

* The second signal of the differential USB data signal from an upstream device
* This pin is connected to the USB-L pins on the connector to the flight computer (J2007)

**XTALIN/CLKIN**

* Connects to one terminal of the 24MHz external crystal

**XTALOUT**

* Connects to the other terminal of the external 24MHz crystal

**PLLFILT**

* PLL regulator filter capacitor
* As the datasheet directs, this pin is connected to ground through a 1.0uF capacitor

**RBIAS**

* This pin sets the USB tranceiver bias
* As the datasheet directs, this pin connects to a 12kOhm resistor to ground (R2065)

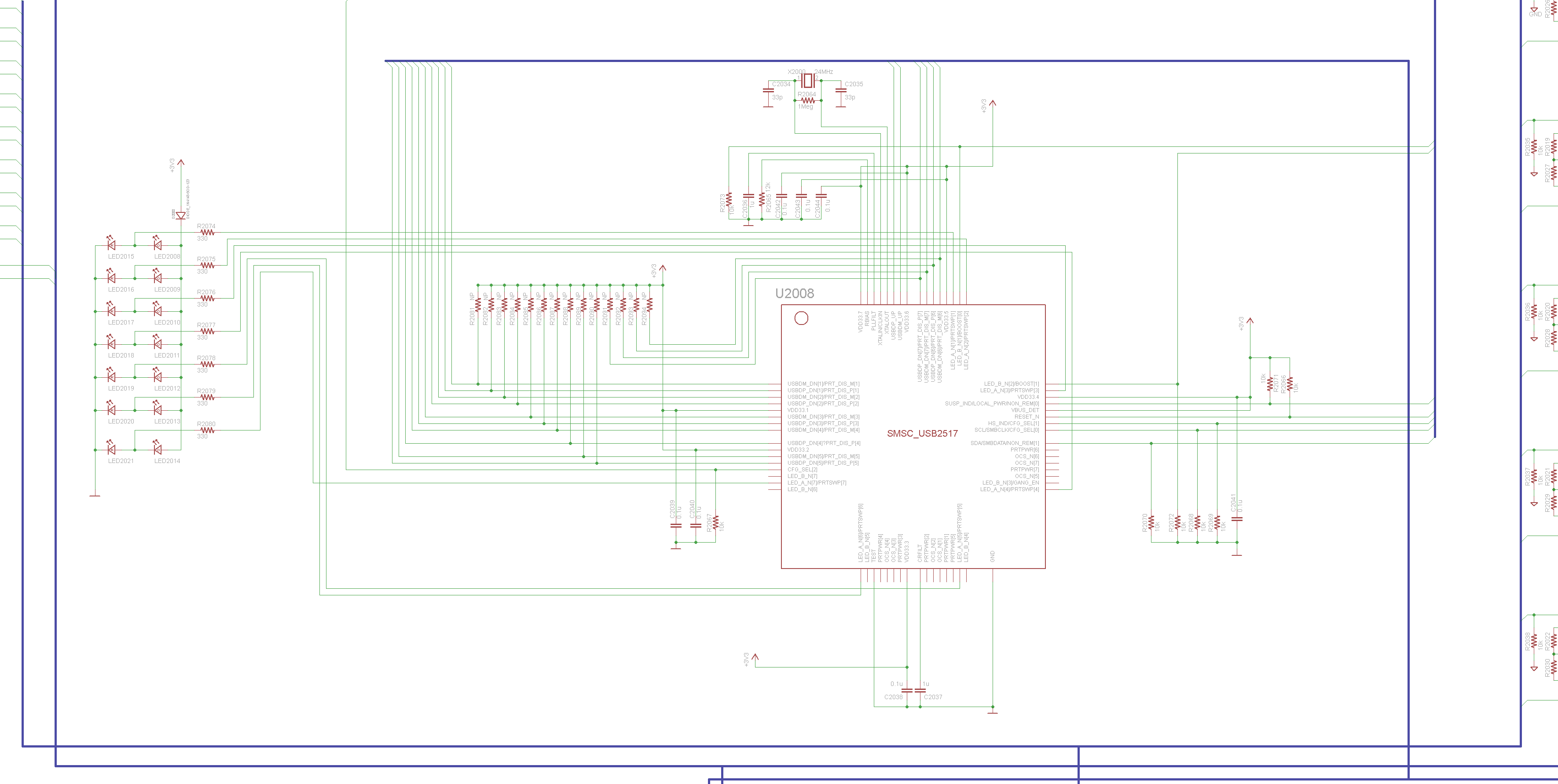
The vast majority of the Hub design was based on references provided from the datasheet. A bird’s eye view of the complete Hub schematic is shown in figure 17 on the following page. Again, for a detailed description of each component used in the design, see Appendix D.

To verify that the Hub design described meets the requirements given we revisit the provided specifications:

*APS USB Hub Verification*

* USB 2.0 compliant with Low, Full and High Speed (480 Mbps)
* Handles 7 downstream devices (devices may be further hubs), and 1 upstream device
* Employs hub status LEDs, which not only indicate the status of each port, but also the speed at which that port is running.

Figure 17: USB Hub Schematic

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### 3.4 APS Battery Selection

#### 3.4.1 Introduction:

During the project the tasks stayed relatively the same, but with changes within each of them. The main areas worked on were the battery and charger for the APS. There were two versions of the charger, one being an IC, and the other being an external charger that would be connected at the launch platform.

*APS Battery requirements*

* SHOULD be a 4-series cell Li battery
* Battery SHOULD cost <500$
* Overall Battery SHOULD have energy-mass density (100,,) W.hr/kg
* Overall Battery energy-volume density SHOULD be (200,,) W.hr/l
* Battery capacity SHOULD be (4,8,) AHr (TODO: TBD on new power budget)
* SHOULD have dimensions less than (,3.0,3.5) inches in the cross sectional plane of the airframe, length (,,10)inches
* MUST have a fuse in the pack before the lead
* Total battery "unplugged" leakage MUST be < C/(1,5,) year rate (e.g. ~ 100 uA for 4 AHr)

#### 3.4.2 Battery packs

With the batteries there were a few specific constraints that could not be ignored. The first being that the battery chemistry needs to be either lithium or lithium polymer; This is because these batteries are smaller, and with other batteries such as the alkaline batteries that are purchased everyday to power such things as flashlights and television remotes, there is a risk of the acid within the battery leaking out, which could have serious consequences is it were to leak out during flight, as it could damage vital components, such as the flight computer. There is also an environmental aspect as the acid is toxic, and would be harmful to the environment if it were to leak out onto the ground.

As part of the research, time was put in to look at various battery types, the first being a battery pack, which consisted of a premade stack of batteries usually associated with model cars or planes. The thought process here related to finding something that was prepackaged and would fit the requirements above. With this prepackaging there would be only 2 wires, the positive and negative poles, at maximum to connect, thus limiting the number of connection that could fail.

In table 1 below you will see a line mentioning an adjustment to the requirements related to the dimensions. Originally the max dimension was 3.5 inches on a given side, however on January 30, 2009 it was decided by the PSAS advisors that the length could be longer than that as it could go down into the rocket, but no more than 10 inches.

**Table 1: Battery Selection Information**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Manufacturer/ model | Capacity (Ah) | | Weight (g) | Dimensions | Price ($) |
| polyquest / PQ-1600LP-4S | 1.6 | 146 | | 3.03 x 1.46 x 1.3002 | 65.99 |
| ThunderPower / LP-TP2000-4SPL | 2 | 159.9 | | 2.561 x 1.97 x .99 | 98.99 |
| Adjustments to dimensions requirements made 01/30/09 |  |  | |  |  |
| Polyquest /PQ-4250LP-4S | 4.25 | 402 | | 5.83 x 1.85 x 1.22 | 136.25 |
| Poly Rc / PQ-4350XP-4S | 4.35 | 436 | | 6.5 x 1.8 x 1.3 | 196.99 |
| Thunder Power / TP4600-4SXL | 4.6 | 457 | | 7.6 x 1.81 x .95 | 161.24 |
| Polyquest model: PQ-5350LP-4S | 5.35 | 469 | | 5.56 x 1.82 x 1.58 | 180.50 |

Upon further clarification it was found that single individual cells, rather than packs would be much better for the design, as we would have control over how they were connected and less chance for error there. As such, research into single cells began. All cells bellow rated at 3.7 V. Table 2 below shows a comparison of different single cell batteries.

**Table 2: Singe Cell Battery Comparison**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Manufacturer/ model | Capacity (Ah) | Discharge | Dimensions  (in) | Weight  (g) | Energy density (Wh/kg) | Price ($) |
| Tenergy / 30512 | 4 | 15C | 5.3 x 1.773 x .26 | 85 | n/a | 51.99 |
| Tenergy / 30502 | 1.25 | 10C | 2.56x 1.379 x .217 | 28 | n/a | 19.99 |
| Panasonic /  CGA103450A | 1.95 | 1C | 1.97 x 1.34 x .42 | 39 | n/a | 13.00 |
| Sanyo / UF103450P | 1.88 | 1C | 1.95 x 1.34 x .37 | 38.5 | 180 | 18.34 |
| BatterySpace.com / PL-896474-2C | 5 | 2C | 2.92 x 2.52 x .35 | 95 | 185 | 24.95 |
| Batteryspace.com /  PL-875055-2C | 2.5 | 2C | 2.167 x 1.97 x .34 | 51 | 181.37 | 13.95 |
| Batteryspace.com /  PL-9059156-1C | 10 | 1C | 6.15 x 2.32 x .35 | 196 | 204 | 32.95 |
| Batteryspace.com /  PL-5467100-2C | 4.25 | 2C | 3.94 x 2.64 x .22 | 85 | 185 | 19.95 |

Based on the specifications, and the research done, it was decided that the Batteryspace.com model:

PL-5467100-2C would be the battery of choice as its size and capacity could create a 8.5 Ah 14.8 V battery when placed in a 4 series, 2 parallel (4s2p) arrangement.

#### 3.4.3 Fuses

Given the battery would need a fuse some research was done, but none were selected.

Here are the models found:

BUSSMAN BK/GBB-17-1-2-R

Littelfuse 456 series

Ferraz Shawmut PCF30-S

As part of the battery research the issues related more to understanding what was needed, as things were labeled battery packs, as such it made sense initially to assume an actual pack rather than individual cells. This was also the first instance where scale of the number of products and suppliers became apparent, as a single Google search for lithium batteries brought back over 3 million results.

### 3.5 APS Battery Charger

*APS Charger Requirements*:

* MUST meet standard lithium charge/discharge safety requirements (thermal, voltage, current, time, fuse)
* MUST be able to charge at (,1C,C/2) rates at internal air temperature of 50 deg C.
* MAY equalize cells up to some small bypass power (e.g., .5W)
* MUST indicate charging status (on/off)
* MAY indicate some kind of charge % (blink rate, color, LED bar graph, etc)

#### 3.5.1 Internal Charger Design

Based on the design used in the past, use of an internal chip mounted charger was selected. An IC charger takes the charge from an external source, such as another battery and transfers that power into the battery within the device, in this case the rocket. However it does this as a specific rate and also monitors how full the battery within the rocket a gotten as well as keeps track of the temperature of the batteries during charging and operation, as overheating could occur during usage. This information is then sent to a microcontroller which depending on how things have been programmed can decide to shut off the charger, or alert the individual operating the rocket that there is an issue.

Given the battery operates at a higher capacity than the batteries used in previous designs, research into different chargers occurred. Factors that needed to be considered included size, charging capability, signaling capabilities, and how well it worked with the umbilical system as they would be linked together, and depending on the charger, there could be additional components, such as switches, needed to join the two parts. Below is a list of the charger ICs researched in the selection process.

**Battery Charger IC Chosen**

Model: LTC 4007

Manufacturer: Linear

Charge Rate: 4A

**ICs Not Chosen:**

Model: MAX8731A

Manufacturer: MAXIM

Charge Rate: 8A

Model: LTC1759

Manufacturer: Linear

Charge Rate: 8A

Model: BQ24705

Manufacturer: Texas Instruments

Charge Rate: 8A

Efficiency: >95%

Model: ISL88731A

Manufacturer: Intersil

Charge Rate: 8A

Model: BQ24751A

Manufacturer: Texas Instruments

Charge Rate: 10A

Efficiency: >95%

Model: BQ24730

Manufacturer: Texas Instruments

Charge Rate: 20A

Model: MAX17005/6/15

Manufacturer: Maxim

Charge Rate: 5A

Model: MAX1909/MAX8725

Manufacturer: Maxim

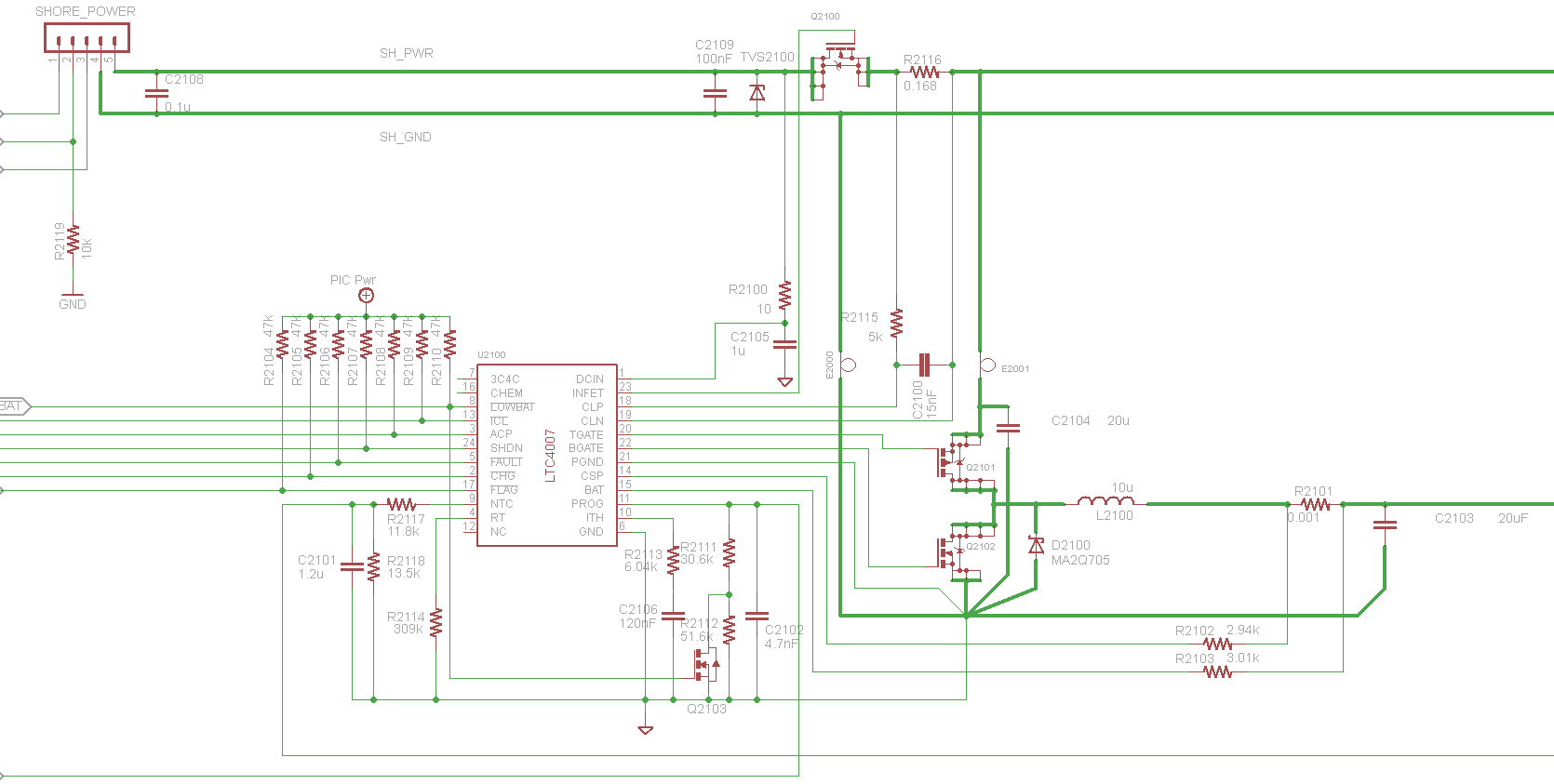
Charge Rate: >4A

Efficiency: >95%

The LTC4007 was chosen as it could charge at 8.5 A, which would make the system charge the battery in an hour if the battery was totally depleted. Another reason for this selection was the input transistor helped with the current control, and helped eliminated some parts within the umbilical system. The other chargers did not have these components, or had some control but needed a bus, or were only useful with a particular type of battery.

This chip had initially been ignored as it was used in the previous design, which operated at a lower capacity. However upon further review of the part, it was found that it could be designed via the networks of resistors, capacitors, and transistors to operate at a higher level than in the previous designs. Also given its use in the past it would seem to be able to deal with the physical demands needed during a launch. Figure 18 below shows the EAGLE schematic for the internal APS battery charger circuit. Parts descriptions for the components used can be found in Appendix E at the end of this report.

Figure 18: Internal Battery Charger Circuit

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#### 3.5.2 External charger:

Near end of project the PSAS decided to look into using an external charger given the capabilities of the charger that they had selected, and space on the board. with an external charger, it performs the same duties as the IC version, but instead of being located on a board, it is attached only at launch via the umbilical system, and detaches at launch. The reason for selecting such a device is that there would not be any need for and on board charger which takes up valuable board space, which was on short demand given the size of other components on the APS board. However even though the charger itself exists outside the rocket there still existed the need for current protection and power switching relating to the charging of the batteries as in the IC design.

Looking at power switches and the internal charger design saw use for switch controller and transistor as they had the range needed, and by using the enable pin to switch, could control via the microcontroller. The first one would be used in relation to the battery during charging and when disconnecting the charger, the other two would be for different loads, and could be removed if no loads, or more added as needed. They are there as an example of what could be done.

With the charger design it was learned that design is ever changing and that knowledge about datasheets was not as good as previously thought, as many hours were spent just looking at datasheets trying to figure out what the datasheet was actually describing, as some have different names for the same pins. Appendix F contains the detailed parts list for the external charger circuitry.

### 3.6 APS Battery Sensor System

#### 3.6.1 Introduction:

As we may all notice, we can check how much power our laptops have by pressing the button on the battery. The amount of power is indicated by the LEDs on the battery. The battery sensor used in the project has the similar function as the LEDs mentioned above. The difference is that instead of monitoring the power, the battery sensor monitors the voltage, current and temperature of the battery packs.

*APS Battery Sensor Requirements*

* MUST monitor charge ("coulomb counter")
* MUST measure pack voltage
* SHOULD monitor the voltage on each cell
* MUST monitor battery pack temperature (MUST be compatible with charging chip)
* SHOULD separate high current connector from sensing connector
* MUST work with 8-cell Li-ion battery (4-cells in series and two cells in parallel)

#### 3.6.2 Battery Sensor System Design

1. Choose the IC chips
2. The only chip that works with 1-10 cells Li-ion Battery is DS2788 from Maxim. DS2788 can monitors the voltage, current and temperature, however, it doesn’t have the feature to monitor the voltage on each cell
3. ISL9208 from Intersil is selected because it can monitor the voltage on each cell and it supports battery pack configurations consisting of 4-cells to 7-cells in series and 1 or more cells in parallel.
4. Features of the selected IC chips
5. DS2788 (1):

* Measures voltage, temperature, current and estimates available capacity for rechargeable lithium-ion (Li+) and Li+ polymer batteries.
* Cell characteristics and application parameters used in the calculations are stored in on-chip EEPROM. The available capacity registers report a conservative estimate of the amount of charge that can be removed given the current temperature, discharge rate, stored charge, and application parameters. Capacity estimation is reported in mAh remaining and percentage of full.
* LED display drivers and a debounced input make display of the capacity information easy. The LED pins can directly sink current, requiring only a resistor for setting the current in the LED display, thus reducing space and cost.
* 14-Pin TSSOP Package

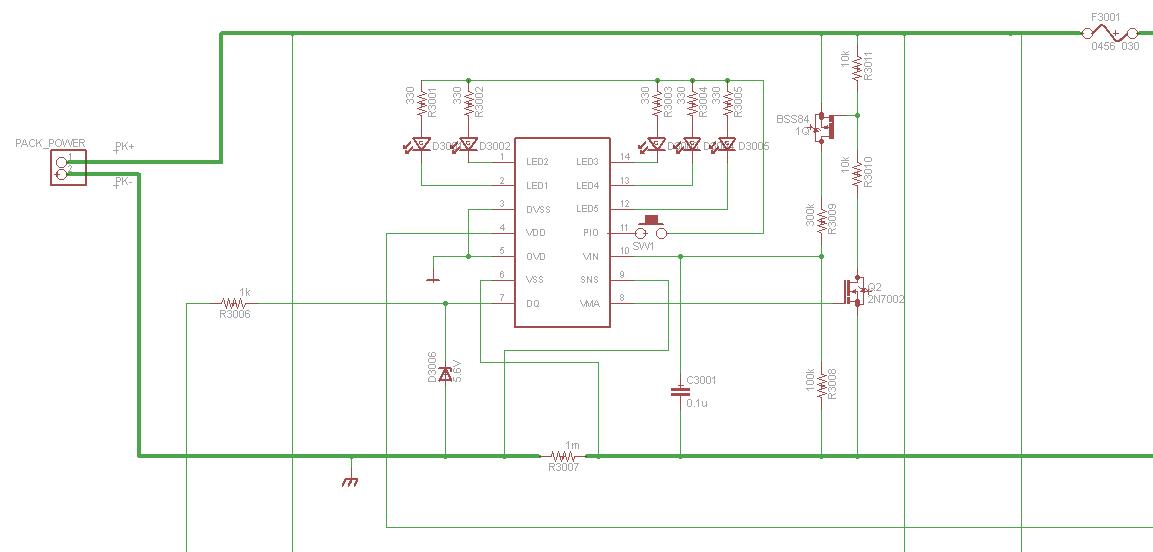
1. ISL9208 (2):

* Supports battery pack configurations consisting of 4-cells to 7-cells in series and 1 or more cells in parallel. (Note: In the application note of ISL9208, it shows the battery connection for battery packs of 4-cells to 7-cells. It also mentions that the battery packs with 4-cells have not been tested. However, it should work with 4-cells battery as well.)
* Provides integral over-current protection circuitry, short circuit protection, an internal 3.3V voltage regulator, internal cell balancing switches, cell voltage monitor level shifters, and drive circuitry for external FET devices for control of pack charge and discharge.
* Selectable over-current and short circuit thresholds reside in internal RAM registers. An external microcontroller sets the thresholds by setting register values through an I2C serial interface. Internal registers also contain the detection delays for over-current and short circuit conditions.
* Using an internal analog multiplexer the ISL9208 provides monitoring of each cell voltage plus internal and external temperature by a separate microcontroller with an A/D converter. Software on this microcontroller implements all battery pack control functionality, except for over-current and short circuit shutdown.
* 32 Ld 5x5 QFN Package

1. The schematics of the battery sensor
2. **DS2788 Block:** Send out the voltage, current, and temperature through the 1-wire interface. Five LEDs indicate the capacity estimation.

* **LED1… LED5:** Display Driver. Connect to an LED connected to VDD for display of relative pack capacity.
* **VDD:** Power-Supply Input. Connect to the RGO pin of ISL9208.
* **DVSS:** Display Ground. Ground connection for the LED display drivers. Connect to VSS.
* **OVD:** 1-Wire Bus Speed Control. Input logic level selects the speed of the 1-Wire bus. Logic 1 selects overdrive (OVD) and Logic 0 selects standard (STD) timing.
* **VSS:** Device Ground. Connect directly to the negative terminal of the battery cell. Connect the sense resistor between VSS and SNS.
* **SNS:** Sense Resistor Connection. Connect to the negative terminal of the battery pack. Connect the sense resistor between VSS and SNS.
* **VIN:** Voltage Sense Input. The voltage of the battery cell is monitored through this input pin.
* **VMA:** Voltage Measurement Active. Output is driven high before the start of a voltage conversion and driven low at the end of the conversion cycle.
* **DQ:** Data Input/Output.
* **PIO:** Programmable I/O Pin.

Figure 19: APS Battery Sensor Circuit



1. **ISL9208 Block:** The device wakes up when a charger is connected to the pack. The main purpose of this block is to monitor the cell voltages and temperature information, and send out the information with I2C interface and through analog multiplexer output. Besides that, the discharge current and charge current of the battery pack are also monitored by the circuit.

#### VC7, CB7... VCELL1, CB1: Cell balance circuit with 4-cell battery. (Note: adding a series resistor on each of the cell inputs reduces the initial current surge through the inputs, but it affects the accuracy of the cell measurements. A series of 15ohms resistor will add about 1mV of error to the cell voltage reading.)

#### DSREF, DSENSE, CSENSE: Monitor the discharge current and charge current by monitoring a voltage across a sense resistor

#### AO: Analog multiplexer output, which is used by an external micro-controller to monitor the cell voltages and temperature sense voltage.

#### TEMP3V, TEMPI: Temperature monitor. TempI pin inputs the voltage across a thermistor to determine the temperature of the cell; TEMP3V pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor.

#### RGO: Regulated output voltage, this pin connects to the emitter of an external NPN transistor and works in conjunction with the RGC pin to provide a regulated 3.3V

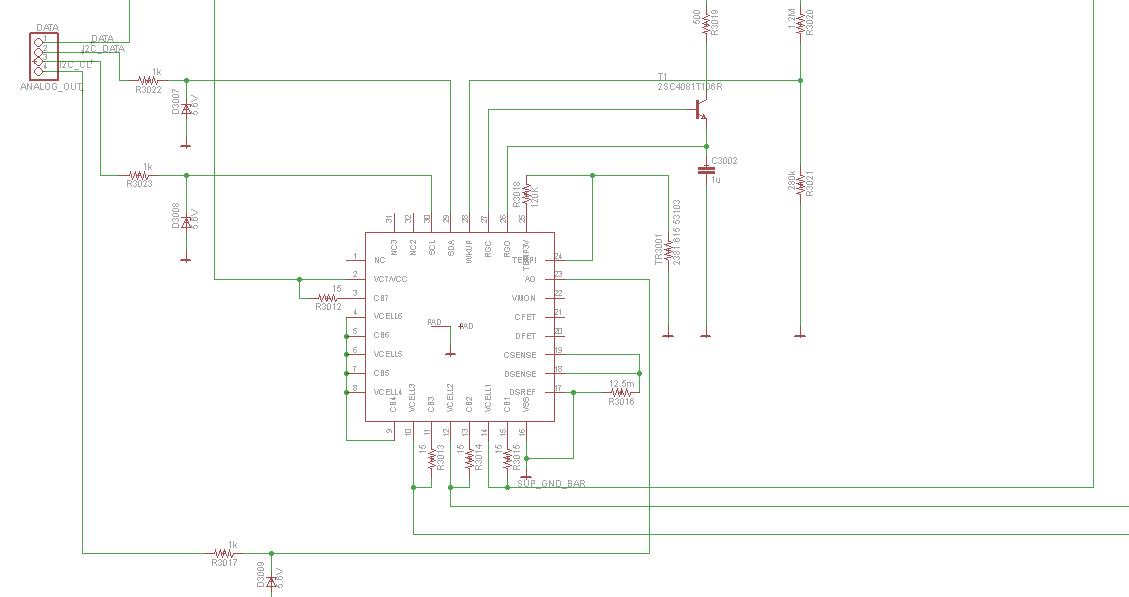
#### RGC: Regulated output control. This pin connects to the base of an external NPN transistor and works in conjunction with the RGO pin to provide a regulated 3.3V. The RGC output provides the control signal for the external transistor to provide the 3.3V regulated voltage on the RGO pin. The 500ohms resistor in the collector reduces the initial current surge when the regulator turns on.

#### WKUP: Wake up voltage. In an active LOW connection (WKPOL = “0” - default), the device wakes up when a charger is connected to the pack. This pulls the WKUP pin low when compared to a reference based on the VCELL1 voltage. Please see the figure 9 of the application note for more information.

#### SDA: Serial Data

#### SCL: Serial Clock

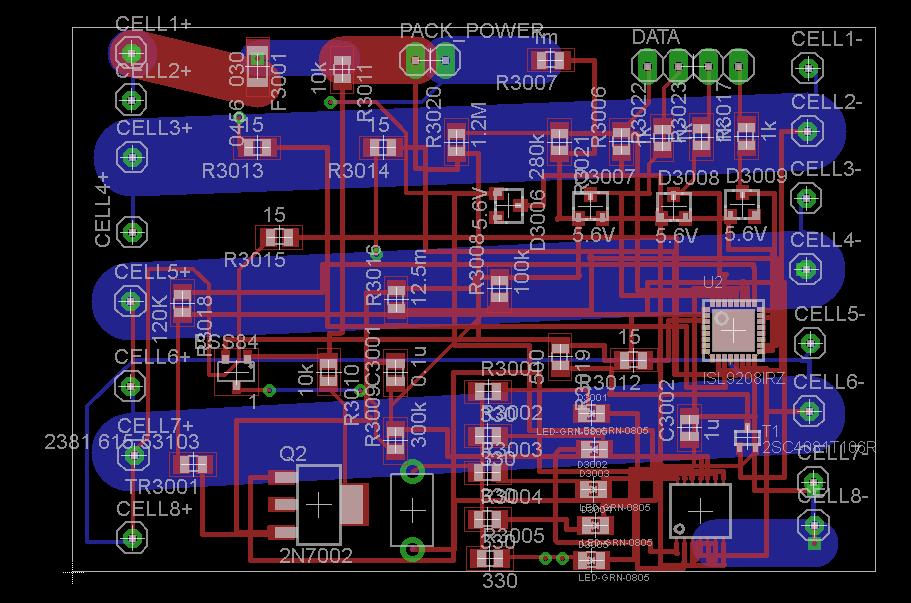
Figure 20: ISL9208 Battery Sensor System block



1. Component Selection: For a detailed description of the components used, see Appendix G at the end of this report.
2. The layout of the battery sensor board

In our project, the battery sensor board is placed next to the eight battery packs. Since the size of the battery pack is large, the eight battery packs are piled up. The battery sensor board is placed vertically to the connector pins from the battery packs. The layout board is shown below in figure 21:

Figure 21: Battery Sensor Board Layout



The battery sensor circuit monitors the voltage, current, temperature and voltage on each cell. The drawback of the circuit is that it contains two types of interfaces: 1-wire interface and I2C interface. Also, in order to simplify the circuit, the over-current protection circuit of ISL9208 is not used; instead, a fuse is placed inside the circuit to obtain the over-current protect function.

### 3.7 APS Analog Pressure Sensor Design

#### 3.7.1 Introduction:

According to the fact that air pressure decreases as altitude increases, a pressure sensor is used inside a rocket to monitor altitude. At sea level, the absolute atmospheric pressure is 101.33 kPa, and at 100,000 feet altitude above sea level, the absolute atmospheric pressure is 1.12 kPa(1). Therefore, in order to monitor the altitude more precisely, the pressure sensor should be able to measure the pressure from 0 kPa to 102 kPa. The pressure sensor previous used is VTI SCP1000. According to the datasheet, if the pressure is between 30 kPa to 120kPa, then SCP1000 can measure the pressure correctly. The purpose of this part of project is to study the functionality of SCP1000 and find an analog pressure sensor that can accurately measure the pressure from 0 kPa to 120kPa.

*Pressure Sensor Requirements*

* MUST have pressure range of 0 - 1 ATM (0 kPa - ~115 kPa, 0 - ~15 PSI) or more
* Absolute pressure (needs onboard reference)
* SHOULD use (,3.3,5) V power supply
* SHOULD use (,10,50) mA current
* SHOULD have single ended analog output OR digital output
* MAY have quick response time < 1 ms (~ KHz of bandwidth)
* MUST have a small package size (0,1,10) cm^3

#### 3.7.2 Pressure Sensor Design

1. Study the functionality of SCP1000 from its datasheet. Features of SCP1000 are listed below(2):

* 30 kPa – 120 kPa measuring range
* Single +2.4 … 3.3 V supply
* Four measuring modes plus power down mode
* Standard digital output: SPI or I2C
* Small package size. Diameter 6.1 mm, height 1.7 mm

1. Write the algorithm for SCP1000 with SPI interface.

In this project, SCP1000 outputs the pressure and temperature data to the microcontroller. Therefore, SCP1000 is configured to operate with active MISO (Master In, Slave Out) , which means that the microcontroller sends in the commands to the pressure sensor SCP1000, and SCP1000 sends back the pressure and temperature data as output. The algorithm written below is based on the specification (3) of SCP1000.

To do that, the following commands need to be sent from the microcontroller:

1. Write 0x09 in direct register 0x02 (ADDPTR)
2. Write 0x13 in direct register 0x01 (DATAWR)
3. Write 0x02 in direct register 0x03 (OPERATION -"write indirect register")
4. Wait for 100 ms

The second step is to read the pressure and temperature data:

1. Read the LSB of the STATUS register (0x07). If the content is '0', then the start-up procedure is finished successfully. Otherwise, re-check the STATUS register after 10ms delay
2. In continuous measurement mode the output data is refreshed after each measurement and the availability of the updated pressure and temperature data is signaled through the assertion of the DRDY pin and a DRDY bit (Bit 5) is set to ‘1’ in the STATUS register (0x07).
3. The selection and activation of the measurement mode is done by writing the corresponding mode activation code in to OPERATION register (0x03); Write "0x09" to the OPERATION register to get "High speed acquisition mode" start (continuous measurement). Use operation 0x00 to stop the continuous acquisition
4. The temperature is stored in the TEMPOUT register(0X21) bits[13:0]
5. The MSB of the pressure data is stored in the DATARD8 (0x1F) register bits[2:0], and the 16 LSB data is stored in the DATARD16 register (0X20)
6. Find another pressure sensor that satisfies all the requirements

ASDX series and ASDX-DO series are the only two series of the pressure sensors that satisfy all the “Must” requirements above. The problem with these two series is that their response time is 8ms, which is larger than 1ms in the requirement. But 8ms is an acceptable value in our project. Therefore, the next step is to decide which series should be used. The comparison between the two series is shown below:

1. In common:

* ASIC-enhanced output
* Wide compensated temperature range from 0 °C to 85 °C
* Available in absolute, differential and gage types.
* Pressure range from 0 psi to 1 psi through 0 psi to 100 psi
* The absolute sensors have an internal vacuum reference and an output voltage proportional to absolute pressure

1. Differences:

|  | **ASDX Series** | **ASDX DO Series** |
| --- | --- | --- |
| Accuracy | Max ±2.0 %V | Max ±2.0 % H full scale |
| Output Resolution | N/A | Typical 12 bits |
| Quantization step | Typical 3 mV | N/A |
| Response time | Typical 8 ms | Typical 8 ms and Max 11 ms |
| I2C compatible protocol | No | Yes |

Note:

* Quantization step is the smallest change in the output voltage given any change in pressure.
* For 12 bits digital output, the smallest change in the output given any change in pressure is 5V/(2^12) = 1.22 mV

The advantages of the digital output series are:

* The output resolution of the digital output is 12 bits, while the quantization step of the analog output is 3mV.
* The response time of the digital output one is typical 8ms with max 11ms, while the analog output one is 8ms with no data about the max response time
* The digital output one supports I2C compatible protocol while the analog one doesn't.

Since the ASDX DO series has better features, we chose the pressure sensor from this series. One of the requirements for the pressure sensor is that it must have pressure range of 0 - ~15 PSI or more. Therefore, ASDX015-DO is selected.

1. Pressure Sensor Test (4)

The giant vacuum chamber in [Dr. Erik Sanchez's lab](http://www.physics.pdx.edu/%7Eesanchez/) at PSU is used to test pressure sensors to near vacuum and outside their usual acceleration and temperature ranges. The testing is handled by PSAS. The results from the test are:

1. The SCP sensor was accurately reflecting the pressure recorded on the pressure gauge, even down to 0.45 kPa.
2. The ASDX did as expected and worked down to 0.45 kPa

Based on the results from the pressure sensor test, both SCP1000 and ASDX DO series can be used to monitor the rocket’s altitude in our projects. The main difference between them is that SCP1000 uses SPI interface while ASDX DO series use I2C. Since the microcontroller we use supports both interfaces, we can use either or both of the pressure sensors.

# 4 Firmware Design

### 4.1 Introduction:

Our general objective was to create firmware to run the APS and all its peripherals. We were to provide for real time data collection and response. In all cases we were to design for safe failure modes, and to design the node to fail gracefully where possible. We were also directed to maintain modularity wherever reasonable to allow for code re-use in other nodes.

Initially, we were to work on the Generic Node software. Our second priority was to work on the software for the Avionics Power System, starting with the APS state machine.

The Generic Node software was required to have:

Error handling

* Error levels: debug, info, warn, error
* Error logs (Sequential error list and error count)
* Error messages (protocol undecided, may be CAN, UART, or USB)

Serial console

* Command interface
* Communication interface to the error logs (request counts, etc)

The Avionics Power System software was required to support:

Power switching to sub-systems

Over-current monitoring

Battery management

* Charge battery
* Read battery voltage and current
* Pack voltage
* Cell voltage
* Charge counting (into capture timer) (charge, amps = charge/delta\_T)
* Never turns off unless physically disconnected from battery

Umbilical

* Monitoring of shore power
* rocketready signal indicates ready for launch (this involves critical safety issues)
* Any node must be able to scrub launch by de-asserting rocketready

APS must have states:

* Sleep
* Wake
* Safe
* Armed
  + Armed must check to see that all is in place for launch.

The nodes were to be built on a “generic” platform, consisting of an ARM7 processor, with peripherals to achieve the required functionality. The processor model was initially the NXP LPC2148, but was later changed to the NXP LPC2368.

### 4.2 Firmware Development Environment

Our software development environment consisted of individual laptops with a Linux operating system (Debian) and a GCC based cross compiler that compiled code to a hexadecimal memory table format. We were also provided a suite of utilities to load files of this format to the microcontroller via JTAG and serial connections. The primary programs in this suite were OpenOCD for the JTAG, and LPC21ISP for the serial programming. Programming via USB was another option that existed, but that we did not explore. Minicom was used in most instances for serial communication, although other options were pursued to ensure correct traffic by sniffing raw serial traffic. Software tracking and versioning was handled with Git.

We were provided development boards for the LPC2148 and later for the LPC2378. Both boards were manufactured by OLIMEX, and the LPC2378 was considered similar enough to the LPC2368 to be used as a development platform. The boards provided pins for access to all of the on-chip peripherals and a majority of the GPIO ports. The boards provided some standard ports, namely serial, USB and JTAG as well as a prototyping area for soldering connections. Limited testing devices were also provided, including buttons, LEDs, and in the case of the LPC2148 a buzzer and potentiometer.

We were also provided with cabling and adapters sufficient to connect to the device via USB, serial and JTAG. Later we were provided with some samples of sensors that the nodes were expected to use.

The software was written to operate within various versions of FreeRTOS, an open source real-time operating system. The main functionality that FreeRTOS provided was that of multi-tasking or time-sharing on the processor.

### 4.3 Software Development

The process of software development began with the installation of the development software, and a thorough understanding of the tools. This process was very detailed and very arduous. The setup of the development software and gaining a working familiarity with it was the largest single expenditure of time.

The cross-compiler suite had a complex net of dependencies, and many of the libraries and functions it required were of specific and deprecated versions of GCC and other software. We required the direct assistance of several technical advisors provided by the sponsor merely to install and configure the cross-compiler.

Much of the initial month of the project revolved around exploring Debian and the compiler suite, learning which tool was best for which portion of the job. The need to select and configure a text editor, the constant review of the correct arguments for shell commands, and unfamiliarity with Linux’ handling of peripherals all had to be dealt with before actual coding could commence. Git was found to be a very powerful tool for collaboration, but also involved a steep learning curve. In this pre-coding period much time was also spent in review of the microcontroller, the layout of the development board, and review of the protocols we expected to need.

Into the third week we were able to load the microprocessor with demo code, and execute it successfully. We then proceeded to obtain the PSAS approved version of FreeRTOS and were able to successfully load it onto the microprocessor via similar methodology. The initial software items were developed for the LPC2148.

The first items of software developed were for reading the GPIO and ADC. This was based off of demo code provided with FreeRTOS, but was expanded such that ADC sampling was provided its own task so it would not be blocked by other communication, and was able to operate as fast as possible. An API existed in the initial version of FreeRTOS that allowed for selection of the port and channel of the ADC to initialize as a single function. The API further provided functionality to read a particular port and channel. The GPIO functionality had a similar API.

The ADC reading was used to set the frequency of a blinking LED, and also was sent via the UART to the console of the laptop. Implicit in this was the use of the GPIO functionality to actuate the LED.

Production of this item largely consisted of understanding the multi-tasking FreeRTOS environment, the provided API, and the layout of the development board. The ADC suite was later expanded to read several ports in series, with the data collected and sent via the UART for the pressure sensor testing.

The next item of software developed was that for the UART control structure. Messages were sent to the console early on via the serial port, but there was no example of the handling of return traffic in the initial demo. Examples were found in other demos, and this code was initially extrapolated to provide an echo of the characters typed back out to the user at the console.

Once the echo functionality had been established, a pattern matching system was developed, such that the application collected characters in an array of up to 127 characters, up to the first carriage return. This collected array was compared with a list of “commands.” If there was an exact match, the command was executed. If the array did not match the commands, and informative error was returned.

This structure was used later in the Error Handling software, and similar structures were used in the pressure sensor testing and also in the APS state machine.

The pressure sensor testing code used all aspects of the developed software to this point, including an SPI protocol suite developed by another team member and not mentioned in this report. Our initial attempts to provide a software suite suitable for the task yielded code too slow and unwieldy to operate within the parameters of the test. Technical advisors provided by the sponsor were able to assist us in bringing our previous code sections together in a cohesive and efficient fashion. This also proved quite useful in the better understanding of the operation of our development environment. The pressure sensor testing code rapidly sampled two analog pressure sensors, two outputs of an analog accelerometer (dual axis), and a pressure sensor communicating over high-speed SPI. The code communicated the data out via the UART to an attached laptop for data recording. The data was sent in packed binary, and unpacked at the laptop to ensure that the data could be read out quickly enough. The program was also controlled over this UART connection, taking direction to start and stop sampling the sensors.

The pressure sensor testing code operated successfully in both vibration and vacuum chamber tests, and allowed for calibration of the sensors.

The I2C interface was expected to be used for one of the pressure sensors in the pressure sensor testing, but the package delivered was analog. The protocol for I2C communication was laid out in an algorithm and then in stub code form. As the necessity was removed, this portion was shelved until after the critical deliverables were met.

A software suite for the protocol was never implemented for either microcontroller, but the stub code and algorithm should allow for an expedited roll-out for either the LPC21xx or LPC23xx platforms.

Error Handling was the next portion of software written. The error handling package provided a series of 128 byte character arrays in which to store the errors in plain text. Plain text was chosen for the simplicity and transparency it would provide to those debugging the node. The cost was the consumption of around 16k of flash on the microcontroller, but this was considered well within acceptable parameter. Errors were listed with an error level in text, and then the error message, with an option for additional error details. Functions were provided such that the error list would be sent out over a serial port if the proper command was received on that serial port. If the program received a separate command it would provide the numbers of errors aggregated so far.

The error handling suite was largely built upon the UART control structure, and handled text in the same fashion. Key differences were the aggregation of strings outside of the UART control task, the specific commands to handle the errors and their related functions, and functions to operate on data outside the scope of the UART control task. Error handling was one of our required deliverables.

The next portion of software dealt with the general node firmware architecture. The task overhead and inter-task communication in FreeRTOS were reviewed and it was decided based on .hex file size growth as additional tasks were added that we should be able to support around 18 tasks without significant additional operating system overhead.

Thus we proposed a node architecture involving a task to handle the FSM containing the state of the node, and also containing the key decision making block of the node, with other tasks to handle the nodes needs grouped on a functional basis. The UART communication would be consolidated to one task, allowing for software flow control and deterministic traffic flow could be more easily assured. Similarly, other interfaces would be consolidated to a given task, one for I2C, and one for SPI. GPIO and ADC handling might be consolidated or spread to several tasks depending on the criticality of the peripheral or duty of the interface. Thusly the priority of the tasks could also be appropriately adjusted.

This portion was largely research, specification and architecture. The assumption is that as the generic node software is expanded, it should grow along these lines for optimal performance and reliability.

Late in the project we were presented with a change of hardware, moving to the LPC2368/78 processors. We were provided LPC2378 processors as a development environment for the LPC2368 processor. At this time we were also migrated to a version of FreeRTOS two major-point releases ahead of the version we had been previously programming for. With our previous experience, we were able to rapidly analyze the new operating system and processor feature sets, noting the critical differences, and begin migrating code.

The GPIO functionality for the LPC2368 was decidedly different than that of the LPC2148, with a greater number of ports and larger total number of GPIO pins. There was no provided API for the GPIO initialization functionality in the new FreeRTOS version.

The first step was to test the GPIO functionality, ensuring both input and output. This was done by using one GPIO pin to read the state of one of the buttons on the development board, and then to use another to set the state of one of the onboard LEDs.

Once proper behavior was assured, a suite of functions were created allowing the easy initialization of GPIO pins. The code was created such that a user defined pre-compiler parameter selects the microcontroller that the code should be created for, ensuring correct operation on both the LPC2368 and the LPC2378 despite their difference in GPIO functionality.

The ADC functionality was reduced to one port in the LPC2368/78, down from two ports in the LPC2148. The number of available channels varied between the LPC2368 and the LPC2378, having 6 and 8 respectively. Again, no API was given for the ADC in the current FreeRTOS version. The procedure to construct the API was similar to that described for the GPIO. The ADC was brought up manually and tested against a potentiometer to assure functionality, and then the API was created using the proven initialization algorithm.

### 4.4 Lessons Learned During Firmware Development:

The biggest hurdle we faced was that of learning our development environment. A lot of time was spent trying to understand the tools, and the errors they generated, or failures that occurred due to their misuse. The UART in particular was made quite difficult by subtle settings in Minicom that led to apparently non-deterministic behavior. This led to several days of troubleshooting before the culprit was discovered (hardware flow control was on.) A lot of time was also spent gaining familiarity with the use of Linux (Debian) as a platform for development environment. Early on we had several strange issues with Debian, and it was decided that we migrate to a release that had been declared stable just a few days before.

We were also far more familiar with development in a Windows environment, and the shift involved a steep learning curve, and a significant amount of research. We found Git to also require a significant amount of experience before it became useful, but we were well aware of the need for version control, and found the time to be well spent

We also faced an unusual amount of issues with hardware. Programming via the JTAG occasionally left the LPC2148 boards in a “hung” state, requiring that they be flashed with a null .hex file via the serial port. The JTAG ports of two of the development boards failed, and while they were under similar circumstance, the actual cause was never determined. We finally settled upon different methodologies that we each found reliable and achieved similarly consistent results

The single most valuable thing we learned was the best practices for this type of build-up. This is to get your development environment up and stable as soon as possible, and then to ensure bi-directional communication to the device, be it over serial, USB or some other protocol. With this in place one can begin to test and troubleshoot the rest of the peripherals, and have in place a structure for debugging errors and feedback. Additionally, in the case of complex bus protocols such as I2C and SPI, it was pointed out that the best methodology is to set up the bus as one expects it should run, and then use an oscilloscope or digital analyzer to read the data off the bus, testing it against the expected bus traffic.

In the end, we were able to meet the basic requirements for the software suite for the generic node and APS as required by the sponsor. While we were not able to provide for much of the additional functionality, we are inclined to look to the rather large scope of the project, and to our lessons learned, and count our successes.

# 5 Project Outcomes and Conclusion

The 2009 PSAS Capstone Project had several goals in redesigning two main components of the LV2c avionics systems: enable a Generic Front End which could be installed on various avionics nodes, including a Highly Available Power supply and a Switching Power Supply; develop an Avionics Power System to distribute power and data signals to the avionics nodes; and provide the firmware foundation to control these various systems and be an autonomous system to provide recovery in case of failure of the flight controller. Various tools and resources were available to the Capstone team, though some were utilized much more effectively than others. Among the noteworthy resources were PSAS member expertise, test hardware, open-source development tools, and finally guidance and help from our PSAS advisors and fellow Capstone team members.

The work performed by the 2006 Capstone team was used as a foundation for the 2009 PSAS Capstone project, and it was improved upon with newer technology and a more encompassing scope. That scope was eventually shaped to focus on the GFE, SPS, APS, and the related firmware. Hardware requirements for these areas were fulfilled except in cases where appropriate parts could not be found or the direction of the project had changed and various requirements with it. In several areas firmware implementation and testing was waiting for finished parts, but general functionality for UART, Error Handling, APS State Machine, and communication to the various required sensors and their communication protocols was established.

Individual portions of the design are over 90% complete, and the post-Capstone task is to combine them into a complete schematic. The finished design would need to be fabricated and tested. At this stage the firmware can be implemented in a more specific manner and tie the system together with the on-board sensors, and other nodes of the rocket including the flight controller. At the conclusion of the Capstone project the firmware is estimated at 50% completion. Estimating the work needed to complete our design scope, the 2009 PSAS Capstone team finished at 60% of completion. Several team members are planning to continue after the official end of the project to complete the design and produce a physical circuit that can participate in future PSAS launches. Consensus among team members was that this project was a very rewarding and enriching experience.

# Appendices:

### Appendix A: GFE Parts Selection and Description

The GFE appendix is broken into three areas, covering the SPS, the HAP, and the Microcontroller respectively.

#### SPS Parts

* LV2C:GFE:U2202 LT3972 Buck Regulator
  + The LT3972 is the heart of the SPS regulator. The LT3972 is a switching regulator from Linear Technologies. It can withstand input voltages as high as 62V which minimizes front end protection circuitry. It is synchronized to the 1.5MHz clock coming from the Micro-controller system.
  + <http://www.linear.com/pc/productDetail.jsp?navId=H0,C1,C1003,C1042,C1032,C1082,P86661>
  + The main function it performs is dropping the 10-20VDC coming in from the APS down to a more workable 5 volts. Specifically in our case it is set for 5.0V. For nodes without the HAP, the SPS can be reconfigured to run at 3.3VDC directly removing the need for the HAP and its associated 3.3V output regulator.
* LV2C:GFE:D2201 Catch Diode
  + Suggested Diode = Digi-Key Part number = PDS340DICT-ND, Diodes-Inc PDS340-13, has the following salient details: -- Vreverse = 40Volts , Iave = 3.0Amps , 6.6mm x 3.6mm footprint.
  + Alternate Diode = Digi-Key Part number = MBRA340T3GOSCT-ND , On-Semi MBRA340T3, has the following salient details: -- Vreverse = 40Volts , Iave = 3.0Amps , 6mm x 3mm footprint. Note apparent junction temperature difference and minimum buy compared to PDS340.
  + Id(avg) = (1.875,,2.14)A
  + Id(avg) = Iout(Vin-Vout)/Vin, Iout=2.5A(max), Vin = (10,,35)V (35V max for IC before shutdown due to OVP), Vout=5V
  + Use a Schottky diode, faster is better for efficiency, 40Vmax is fine since the OVP will shutdown the IC from 35V to 62V, beyond that the diode is likely to be the least of the worries, as the LT3972 will have perished.
* LV2C:GFE:D???? Reverse Flow Diode (removed expect Q2250 to handle this job, no need for the extra loss it would introduce.)
  + This diode is in place to prevent a shorted input from drawing current in the reverse direction through the SPS and draining the battery. Utilizing the same part as the catch diode.
  + Use a Schottky diode, faster is better for fault protection, 40Vmax is overkill as the battery has a maximum voltage below 5Vdc, but is good for protection against a reversed input as well. Ideally this diode should create as little voltage drop as possible in the forward direction to minimize impact to operating efficiency.
* LV2C:GFE:R2202 Frequency Set Resistor Rt
  + 26.7k Ohms
  + When Sync to 1.5MHz is desired, use the table value for 1.5MHz - 20%, or 1.2MHz.
  + For simulation use 20.2k ohms, this results in an operating frequency of 1.49MHz.
  + This resistor is not used or present in the final design (therefore no part number) the pin is connected to a clock for sync.
* LV2C:GFE:R2204 Soft Start Resistor
  + 500k ohms
  + Works in combination with the Soft Start Capacitor below.
* LV2C:GFE:R2205 Feedback resistor R1
  + suggested Resistor: Digi-Key Part Number = RHM536KCCT-ND, Rohm = MCR10EZHF5363, 536kOhm, 1%, 0805, thick film.
  + 532.911k ohms, use 532k ohms.
  + R1=R2((Vout/0.79V)-1 , where R2=100kohms, Vout=5Volts (chosen as Vin for the Charger of the HAP)
  + Could use 560k, but then R2 has to be 105k ohms.
* LV2C:GFE:R2206 Feedback resistor
  + 100k ohms
  + This component value was chosen from the reference design.
  + It needs to be big enough to draw very little current through the feedback loop and still feed the appropriate voltages to the feedback error amp and the power good error amp.
* LV2C:GFE:C2201 Input Capacitor Cin1 (OK to place slightly further from the IC)
  + Per Tim, using a physically large 10uF is fine, but then add a physically small 1uF cap in very close.
  + Suggested Capacitor = Digi-Key Part Number = 587-2247-1-ND , Taiyo Yuden = UMK325BJ106KM-T , 10uF , 50Volt, 20% , Ceramic , 1210 , X5R
* LV2C:GFE:C2202 Input Capacitor Cin2 (Place as close to the IC as possible)
  + Suggested Capacitor : Digi-Key Part Number = 490-3909-1-ND , Murata = GRM31CR72A105KA01L , 1uF , 100Volt, 10% , Ceramic , 1206 , X7R
  + 15uF (could be in range of (10,,20)uF)
  + Xc = -j.01 ohms = 1/jwc , w = 2pi \* 1.5MHz, c=10uF
  + So long as Xc is small at the switching frequency this cap will work, any cap in the range is fine, but the smaller they are the closer they need to be to the IC and the catch diode in order to effectively handle the EMI from the switching.
  + Watch out for Ringing during hot plugging, the cap needs to be able to withstand the full 62V that the LT3972 can during faults and plug in ringing.
  + Use types X5R and X7R, DO NOT USE type Y5V!! (warning per data-sheet)
* LV2C:GFE:C2203 Frequency Compensation Capacitor
  + Suggested Capacitor = Digi-Key Part Number = PCC681BNCT-ND , Panasonic-ECG = ECU-V1H681KBN , 680pF , 50V , package = 0805.
  + Chosen as 15k ohms and 680pF from the reference schematic and the data-sheet.
  + Need help figuring these out.
* LV2C:GFE:C2204 Boost and Bias Capacitor
  + Suggested Capacitor = Digi-Key Part Number = PCC1832CT-ND , Panasonic-ECG = ECJ-2YB1E224K , 0.22uF, 25V , package = 0805.
  + 0.22uF
  + This is set at 0.22uF per figure 5A in the data sheet. So long as the input voltage remains above 7.5V the boost/bias considerations appear minimal as there should be plenty of voltage available to successfully start the IC.
* LV2C:GFE:C2205 Output Capacitor
  + Suggested Capacitor = Digi-Key Part Number = 587-2086-1-ND , Taiyo Yuden = TMK325BJ226MM-T , 22uF , 25Volt, 20% , Ceramic , 1210 package , X5R (Use of this part allows for a shorted switch and is the same part as the suggested input capacitor which is available through Digi-Key in lots of 10)
  + Alternate Capacitor = Digi-Key Part Number = 445-3945-1-ND , TDK = C3225X7R1C226K , 22uF , 16Volt, 10% , Ceramic , 3.2mm x 2.5mm , X7R
  + Alternate Capacitor = Digi-Key Part Number = 478-4594-1-ND , AVX = 1210YC226MAT2A , 22uF , 16Volt, 20% , Ceramic , 3.2mm x 2.5mm , X7R
  + 13.3uF minimum
  + Cout = 100/(Vout\*f(sw)), Vout=5V, f(sw)=1.5MHz
  + Ensure that ESR is as low as possible to maximize efficiency (0.05 ohms or less)
  + Look for High performance electrolytic or Tantalum caps
  + Try to use type X5R or X7R
* LV2C:GFE:C2225 Soft Start Capacitor
  + Suggested Capacitor = Digi-Key Part Number = PCC1840CT-ND , Panasonic-ECG = ECJ-2YB1H104K , 0.1uF, 50V , package = 0805.
  + Choose a large RC time constant to minimize voltage overshoot and reduce Imax for the switch at startup. Choose resistor to supply 20uA when RUN/SS is at 2.5V.
  + Want (3.75k, 585k, 875k) ohms for Vin = (10,14.2,20). 500k worked fine in LT-Spice and is the value chosen. As for the cap, it shows .22uF on the reference design, but won't run the system with that value in LT-spice, choosing 0.1uF as in the test fixture for the LT3972 works fine in the simulation and is the chosen cap value.
* LV2C:GFE:L2201 Inductor
  + Suggested Inductor = Digi-Key Part number = 513-156-1-ND, Coiltronics DR74-6R8-R, has the following salient details: -- 6.8uH, Irms = 2.60Amps , Isat = 3.67Amps , DCR = 0.0418Ohms , Shielded , 8mm x 8mm x 4.25mm , Surface Mount.
  + 5.9uH min
  + Per data-sheet, start with di/dt for L and use dI= 1A = 0.4(Ioutmax) , Ioutmax=2.5A
  + Ipeak must be lower than Ilim (the switch current limit)
  + I(L-peak)= 3A = Ioutmax + dI/2 , Ioutmax = 2.5A, dI = 1A
  + This is good as Ilim ranges from (5.5A to 4.5A) and is always greater than 3A.
  + check ==> Ioutmax = Ilim-dI/2 = 4A , Ilim(worst case) = 4.5A, dI = 1A, So Ioutmax is at worst 4A, resulting in a value that is still above 3A, this is good.
  + Largest dI occurs at max Vin, choose L using the following formula:
  + L=[(Vout+Vd)/(Fsw*dI)]*[1-((Vout+Vd)/Vinmax)], Vout=5V, Vd=0.4V, Fsw=1.5MHz, dI=1A, VinMax = 20V (possibly 30V during failures?)
  + L=5.2uH for Vin = 20V, or L=5.9uH for Vin = 30V
  + Larger values are OK as they will only make dI smaller resulting in improved system responses.
  + RMS rating of L must be greater than Imax = 2.5A
  + Saturation current should be about 30% higher, Isat = 3.25A, but want Isat above 5A during startup, shorts, Over Voltages, and other failures.
  + To keep efficiency high, DCR should be kept below 0.1 ohm.
  + To minimize EMI, use a shielded toroid with a ferrite core.
  + Again, larger L is good since they should have better DCR values, smaller ripple current (dI), and an easier time keeping out of discontinuous mode, but the physical size will be a limiting factor.
* **Legacy devices:** This category includes much of the front-end protection circuitry (Capstone 2006 Frontend Passive Block) and includes devices that have carried over from the 2006 capstone design, often with few or no changes.
* LV2C:GFE:U2250 [Capstone2006 designation: U250]
  + Part Description: MAX5902AAETT +72 V, SOT-23, Simple Swapper How-Swap Controller. Ordered samples from vendor, no Digi-Key. http://pdfserv.maxim-ic.com/en/ds/MAX5902-MAX5903.pdf.
  + Purpose: This hot-swap controller IC serves two purposes: (1) circuit-breaker and (2) the first stage of UVLO protection. The version we chose had a input voltage range of +9 V to +72 V, a 300 mV circuit-breaker threshold voltage, limited inrush current ("soft start") and was an automatic retry circuit-breaker. It also had a built-in thermal shutdown and active low power good (!PGOOD) indicator output pin. The device needed a UVLO resistor divider network (R2250, R2251) and an external PMOSFET (Q2250) switch. There are four events which will cause Q250 to turn off: (1) if there is undervoltage at the input, (2) if there is overcurrent, (3) if the die temperature exceeds +125 C and (4) the ON/!OFF pin 6 is forced low for at least 10 ms. See the MAX5902 datasheet.
  + Specifications/ Calculations: The reasons we chose the 300 mV automatic retry circuit breaker version was that we wanted the SPS to be able to recover from a fault condition by itself and we expect that the nominal load current will not be very close to the 400 mA maximum limit but closer to 300 mA or less. Hence steady-state currents in the range of 400 mA to 500 mA qualify as an overcurrent event and should be detected. To avoid wasting power dissipated by Q220's RDS(on) and R2252, those values should be kept low, therefore the voltage across them should also be low and the 300 mV threshold version satisfied that. Upon power up U2250 keeps Q2250 off and if trigger events (1) and (2) are non-existent, then it gradually turns Q2250 on to saturation in approximately 150 ms. The drain of Q2250 is gradually enhanced at a rate of about 9 V/ ms. This start sequence limits the inrush current giving some "soft-start" protection to its load. Once all transients are gone before the 150ms time period and Q2250 is fully saturated, U2250's circuit-breaker functionality comes up and monitors the Vds of Q2250 between pins 1 and 2. Before this initial power up 150 ms period there is no circuit-breaker functionality. If any one of the 4 trigger events occurs U2250 will turn Q2250 off, de-assert !PGOOD (output a logic high) and reinitiate the start sequence given that the trigger event(s) disappears during the 150 ms period, if not the 150 ms period will repeat. There are two typical turn off times regarding Q2250: 10 ms and 4 us. If there is an ON/!OFF or UVLO trigger event, they need to exist for 10 ms before U2250 turns Q2250 off, which will take an unspecified amount of time. If there is an overcurrent or temperature trigger event, then Q2250 is turned off in 4 us. If the trigger events disappear after Q2250 turns off within 150 ms, then the normal start sequence is reinitiated. Since the purpose of U2250 was to be a circuit-breaker we decided not to use the ON/!OFF pin to turn Q2250 off via any SPS feedback. Only an UVLO condition would be a trigger event. The UVLO threshold was specified as 9 V. See R2250 and R2251. This meant that when a trigger event other than a UVLO condition happens, U2520 would turn Q2250 off in 4 us and would reinitiate the start sequence after a trigger event free 150 ms time period. We needed a way for the LPC2368 (U2201) microcontroller to turn off the SPS, so we connected a logic level NMOSFET (Q2282) to a GPIO pin and connected the drain of Q2282 to the ON/!OFF pin of U2250. Also we connected the active low !PGOOD pin to another GPIO pin for monitoring and/or interrupt purposes. See the GLUE Logic section regarding U2280 and Q2282. See R2253 and Q2251 for the "overvoltage to overcurrent" trigger event emulation. One bad thing that we did not like was the relatively high supply current of U2250 being 1 mA to 2 mA. We believe that U2250 will draw the most current from the power bus when the SPS is in a standby/shutdown mode. NOTE: According to the MAX5902 datasheet there are multiple package options for the different versions of the MAX5902: a TDFN and SOT23 package. All SOT23 packages have the specification that, "This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of solder profiles recommended in the industry standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.", which may or may not present a problem.
  + Changes from LV2B to LV2C: Part number only. Part must still be ordered outside of Digi-Key (vendor still shows samples in stock)
* LV2C:GFE:U2251 [Capstone2006 designation: U251]
  + Undervoltage/Overvoltage Protection (U2251)
  + Part Description: Nanopower Push-Pull Output Comparator with Voltage Reference, 1.8 V < Vin < 5.5 V, SOT-23-6, Tape & Reel (TR), RoHS Compliant, Texas Instruments, TLV3012AIDBVT (Digi-Key p/n 296-16830-2-ND $262.50/2250) NOTE: Ordered samples from vendor no Digi-Key. http://focus.ti.com/lit/ds/symlink/tlv3012.pdf.
  + Purpose: This comparator compares the specified divided SPS output voltage (see R2254, R2255) to its internal reference voltage (1.242 V) for an overvoltage trigger event at the SPS output. It is powered by a secondary supply consisting of CR2250 and C2250. Also it has a pseudo low-pass filter consisting of C2251 and its output (pin 1) with the input being pin IN+ (pin 3). See CR2250, C2250 and C2251 respectively.
  + Specifications/ Calculations: We wanted a low power push-pull output comparator to get rail to rail output swing (approximately 200 mV to 3.1 V) and have reasonable switching and rise/fall times, on the order of several microseconds and nanoseconds respectively. We tied the IN- pin (pin 4) to the internal reference voltage REF pin (pin 5) which will be compared to the divided SPS output voltage at its IN+ pin (pin 3). See R254, R255 and C2251. The "undervoltage" protection is actually provided by CR2250 and C2250 where U2251 will remain powered for a specified amount of time if the +3.3 V SPS output rail drops. See CR2250 and C2250.
  + Changes from LV2B to LV2C: Part number only, order from vendor, not Digi-Key.
* LV2C:GFE:CR2250 [Capstone2006 designation: CR250]
  + TLV3012AIDBVT "Secondary Power Supply" Schottky Diode (CR2250)
  + Part Description: 30 V, 1.5 A, 4 ns, New MiniPower 2P, Cut Tape, RoHS Compliant???, Panasonic - SSG, MA2Q70500L (Digi-Key p/n MA2Q70500LCT-ND $0.83/1) http://www.semicon.panasonic.co.jp/ds/eng/SKH00017BED.pdf.
  + Purpose: CR2250 and C2250 form U2251's power supply. This diode prevents C2250 from discharging anywhere but to the V+ supply pin of U2251. U2251 is indirectly powered by the +3.3 V SPS rail. Pin 6 (V+) of U2251 will be charged to a value very close to the +3.3 V SPS rail. As U2251 draws more current when needed and its V+ voltage drops CR2250's Vf below the SPS voltage CR2250 will re-charge C2250. Therefore the average DC current through CR2250 is not easily calculable but will be on the order of tens to hundreds of uA. Schottky diodes were chosen for their fast switching and reverse recovery times. In response to a overvoltage event at the +3.3 V SPS output, U2251 will output a logic high and turn Q2251 on which will cause an overcurrent event at U2250 which will in response turn Q2250 off thus circuit breaking the bus rail from the SPS and the +3.3 V SPS output voltage rail will go to zero. That is the sequence of events without delay times. This is the way U2251 emulates an overcurrent event from an overvoltage event.
  + Specifications/ Calculations: CR2250 has a low forward voltage and U2251 has an input voltage supply range of 1.8 V to 5.0 V so when the SPS voltage is being brought up C2250 is being charged through CR2250 leaving the voltage of SPS minus the Vf of CR2250 at pin 6 (V+) of U2251: V+ = 3.3 V - 0.05 V = 3.25 V (approximately). See the first graph on page 2 of the MA2Q705 datasheet given that the steady state nominal forward current through CR2250 < 1 mA. See C2250.
  + Changes from LV2B to LV2C: Part number only, this is another Digi-Key non-stock part. It will have to be re-specified or ordered from another vendor.
* LV2C:GFE:Q2250 [Capstone2006 designation: Q250]
  + Part Description: -60 V, -3 A, SOT-23-6, P-Channel MOSFET, Cut Tape, RoHS Compliant, Zetex Inc, ZXMP6A17E6TA (Digi-Key p/n ZXMP6A17E6CT-ND $0.75/1) http://www.zetex.com/3.0/pdf/ZXMP6A17E6.pdf.
  + Purpose: This is the external PMOSFET of U2250 which will turn off given that there is one or more of the four trigger events as described earlier. See U2250. U2250 uses the RDS(on) of the saturated Q2250 as a current sense resistor which generates a Vds voltage which is detected across the Vs (Pin 1) and DRAIN (Pin 2) pins and if it is greater than some threshold voltage, U2250 will switch Q2250 off thus breaking the circuit.
  + Specifications/ Calculations: The maximum SPS output current specified was 400 mA. There are three circuit-breaker threshold voltage versions of U2250: 300 mV, 400 mV and 500 mV. For certain reasons the 300 mV threshold part was chosen. See U2250. Therefore the RDS(on) of the PMOS should be around 300 mV / 400 mA = 0.75 ohm. We used a value of 1 ohm. See R2252. Even though the PMOS is used as a switch (cutoff and saturation) and not an amplifier (cutoff, triode and saturation) we wanted to remove dependence of U2250's threshold voltage detection from the less precise RDS(on) of Q2250 and to a more precise sense resistor. Therefore we added a current sense resistor (R2252) in series with the drain of Q2250 to produce a circuit-breaker resistor, Rcb, which is the series combination of Q2250's RDS(on) and R2252 between the two pins 1 and 2 of U2250. We chose a PMOS with a low RDS(on) compared to the needed calculated value needed to trip the circuit-breaker thereby making R2252 close to Rcb in value. Therefore Q2250 is used mostly as a switch and the voltage drop across R2252 is used to trigger the switch. See R2252. The breakdown voltage of Q2250 has to be greater than 20 V and should have a low "turn on" capacitance. We do not care so much about the Vt but it does affect the "turn on" capacitance but these factors were not considered.
  + Changes from LV2B to LV2C: Part number only. Price has gone down slightly at Digi-Key to $0.75
* LV2C:GFE:Q2251 [Capstone2006 designation: Q251]
  + Part Description: 100 V, 170 mA, RDS(on) = 10 ohm @ Vgs = 4.5V, SOT-23, Cut Tape, RoHS Compliant???, N-Channel Logic-Level MOSFET, Infineon Technologies, BSS123E6327 (Digi-Key p/n BSS123INCT-ND $0.36/1) http://rocky.Digi-Key.com/WebLib/Infineon/Web%20Data/BSS123.pdf.
  + Purpose: This is a logic-level NMOSFET. When an overvoltage at the +3.3 V SPS output occurs, U251 will output a logic high turning Q251 on and thus conducting current through R253. The current flowing through R253 also flows through Rcb and its magnitude is dependent on the value of R253 and the bus voltage at the time (nominal value of 16.8 V). When there is no overvoltage at the +3.3 V SPS output U251 outputs a logic low thus keeping Q251 off.
  + Specifications/ Calculations: Since the gate of this FET would be driven by the output of a comparator in U251 it would be best for the FET to be a logic-level device. Other concerns was for the drain-source breakdown voltage to be higher than 30 V as the highest possible DC value the bus voltage rail would be is 20 V.
  + Changes from LV2B to LV2C: Part number only. Original Part is non-stock, call to order at Digi-Key. Should be re-sourced re-specified, or ordered as a vendor sample.
* LV2C:GFE:Q2282 [Capstone2006 designation: Q282]
  + Part Description: Logic level N-channel mosfet, 100V, SOT23, Fairchild p/n: BSS123 (Digi-Key p/n: BSS123NCT-ND $0.29/1)
  + Purpose: This Nmosfet allows a Microcontroller GPIO pin to activate the shutoff of U2250 (circuit-breaker) resulting in a disconnection of the APS supply to the SPS.
  + Specifications/calculations: See the GLUE logic section of Capstone2006 for detailed explanation of this part.
  + Changes from LV2B to LV2C: Part number only. Still available through Digi-Key.
* LV2C:GFE:TVS2201 [Capstone2006 designation: TVS200]
  + Part Description: 18 V, SMB, Unidirectional, Cut Tape, RoHS Non-Compliant, Diodes Inc, SMBJ18A-13 (Digi-Key p/n SMBJ18ADICT-ND $0.89/1) http://www.diodes.com/datasheets/ds19002.pdf.
  + Purpose: A transient voltage suppressor (TVS), this "zener like" diode protects the SPS (specifically U2202) in the event of an overvoltage at the input.
  + Specifications/ Calculations: It should have a breakdown voltage of about 20 V (unlikely maximum bus voltage) and a current carrying capacity greater than the fuse rated current. It should have a fast response time and be unidirectional. In the event of a sustained overvoltage at the input the only allowable part which can be destroyed is the fuse, F200. That is what we want.
  + Changes from LV2B to LV2C: Part number. The original capstone2006 part is no longer available in Digi-Key. Re-specify or find new vendor. One suggested replacement is B72500D200A60V7 (Digi-Key p/n: 495-3413-1-ND $0.20/1) http://www.epcos.com/inf/75/ds/cd\_standard.pdf This is a simple Zener type ESD suppressor in an 0603 package.
  + Another replacement possibility is: V2F118C400Y1FDP, Digi-Key p/n:478-2486-1-ND. The difficulty here is that new replacement doesn't handle the current that we are looking for, it maxes out at 1A and would blow before the fuse.
  + A final possibility, as the LT3907 is capable of withstanding up to 62V, it could be argued to simply not populate this part, though some ESD protection would be nice.
* LV2C:GFE:F2201 [Capstone2006 designation: F201] Node Power Supply Fuse
  + Part Description: 2000 mA, 63 V, 1206, Fast Acting Short Time Lag, RoHS Compliant, TYCO Electronics, 1206SFF200F/63-2 (Digi-Key p/n 1206SFF200F/63CT-ND $0.46/1) http://documents.tycoelectronics.com/commerce/DocumentDelivery/DDEController?Action=srchrtrv&DocNm=SCD25801&DocType=CD&DocLang=EN
  + Purpose: This fuse protects the SPS from currents greater than 2000 mA. Its direct purpose however is to protect the power bus from a short circuit fault on the SPS side.
  + Specifications/ Calculations: Since the specified maximum SPS current is 2000 mA we chose a fuse rated at 2000 mA. The opening time for the fuse according to its datasheet is .05 s at a current of 8 A, or 5 s at 5 A. Currents of 2 A or below are 4 hours minimum, therefore this fuse will only protect the SPS or power bus from gross currents due to some fault on either side (power bus or SPS) and not to keep the SPS output current within spec, that is U250's job.
  + Changes from LV2B to LV2C: Part number. New value reflecting the higher current rating of the updated SPS.
* LV2C:GFE:R2218 [Capstone2006 designation: R215] Chassis Ground to Node Ground isolation resistor
  + Part Description: 100 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant, Rohm, MCR10EZHF1003 (Digi-Key p/n RHM100KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R2218 provides a DC path from the SPS ground to chassis ground. See page 29 of the CAN Node Switch Mode Power Supply (SPS) (200) section in the Component Design for LV2 Power Electronics (Except Main Battery) engineering design notes.
  + Specifications/ Calculations: 100 kohm worked.
  + Changes from LV2B to LV2C: Part number only. No recognized need for other changes.
* LV2C:GFE:R2250 [Capstone2006 designation: R250]
  + Part Description: 61.9 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Rohm, MCR10EZHF6192 (Digi-Key p/n RHM61.9KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R2250 is part of the UVLO resistor divider of U2250.
  + Specifications/ Calculations: The UVLO voltage was specified to be 9 V. See page 8 and Figure 3 in the MAX5902 datasheet. Letting R251 = 10.0 kohm and using the typical value of Von/!off = 1.26 V, the UVLO formula from page 8 in the datasheet is R250 = R251 \* ((VUVLO / (Von/!off)) - 1) = 61.4 kohm. The closet standard value was 61.9 kohm.
  + Changes from LV2B to LV2C: Part number only.
* LV2C:GFE:R2251 [Capstone2006 designation: R251]
  + Part Description: 10.0 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Rohm, MCR10EZHF1002 (Digi-Key p/n RHM10.0KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R2251 is part of the UVLO resistor divider of U2250.
  + Specifications/ Calculations: R251 was specified to be 10.0 kohm. See page 8 and Figure 3 in the MAX5902 datasheet.
  + Changes from LV2B to LV2C: Part number only.
* LV2C:GFE:R2252 [Capstone2006 designation: R252]
  + Part Description: 0.82 ohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Panasonic - ECG, ERJ-6RQFR82V (Digi-Key p/n P.82DCT-ND $2.10/10) http://www.panasonic.com/industrial/components/pdf/AOA0000CE3.pdf.
  + Purpose: This resistor dominates the circuit-breaker resistor's (Rcb) value. It is in series with the drain (hence RDS(on) of Q2250 to make up Rcb. The voltage drop across it is used to detect an overcurrent event given that it is greater than 300 mV. See Q2250 and U2250. Note: This value may change due to board level testing results.
  + Specifications/ Calculations: Since the typical value of RDS(on) of Q2250 is 0.125 ohm and Rcb was about equal to 1 ohm, R2252 = Rcb - RDS(on) = 0.875 ohm. The closet standard value was 0.82 ohm. Given this value of Rcb and the circuit-breaker trip threshold voltage of 300 mV, the maximum SPS current which can be drawn before an overcurrent event is Imax = 300 mV / (0.125 ohm + 0.82 ohm) = 317 mA which is under the specified maximum SPS current spec.
  + Changes from LV2B to LV2C: Part number only. Probably need to recalculate the default value, but it is likely to be changed during board level testing regardless.
* LV2C:GFE:R2253 [Capstone2006 designation: R253]
  + Part Description: 47.0 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Rohm, MCR10EZHF4702 (Digi-Key p/n RHM47.0KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R253 along with Q2251 will "emulate" an overcurrent trigger event as seen by U2250 when an overvoltage at the SPS output trigger event as seen by U2251 occurs. See Q2251. When the SPS +3.3 V output rises above a certain threshold, the output of U2251 goes high, turning Q2251 on. When this happens it pulls pin 2 of U2250 very close to ground and current flows through R253 and Q251. Now that pin 2 is close to ground and pin 1 is normally close to the power bus voltage this is much greater than 300 mV this causing an overcurrent trigger event for U2250. R2253 limits the extra current pulled through Q2251 when it is turned on.
  + Specifications/ Calculations: In normal SPS operation, the voltage drop across Rcb will be less than 300 mV and R2253 is connected to the high impedance pin 2 of U2250 so no current flows through it. If there is an overvoltage trigger event at the SPS output, Q2251 is turned on conducting current through R2253 which will have a voltage drop of approximately 300 mV less than the power bus voltage: VR2253 = 16.8 V - 300 mV = 16.5 V. This results in a current boost of about IR2253 = 16.5 V / 47 kohm = 351 uA which is negligible.
  + Changes from LV2B to LV2C: Part number only.
* LV2C:GFE:R2254 [Capstone2006 designation: R254]
  + TLV3012AIDBVT UVLO Lockout Resistor Network (R254, R255)
  + Part Description: 18.2 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Rohm, MCR10EZHF1822 (Digi-Key p/n RHM18.2KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R254 along with R255 form a voltage divider with respect to the +3.3 V SPS output rail. When there is an overvoltage at the +3.3 V SPS output the voltage at the IN- pin (pin 4) of U2251 will be greater than the internal reference voltage of U2251 (typically 1.242 V) and will result in the comparator in U2251 outputting a logic high value. When the SPS output is below a certain threshold the input voltage (pin 4) to U2251 is less than the internal reference voltage and the comparator's output is a logic low.
  + Specifications/ Calculations: From the LPC2148 datasheet the maximum supply voltage it can handle is 3.6 V therefore we specified that if the +3.3 V SPS output was to reach 3.5 V we would want this to qualify as an overvoltage trigger event. Since we have been using several 10.0 kohm resistors we specified R255 to be 10.0 kohm. Therefore using the overvoltage trigger event value to be 3.5 V and the compared voltage to be 1.242 V we solved for R254: 1.242 V = (3.5 V \* R255)/ (R255 + R254) and solving for R254 = 18.18 kohm. The closet standard value was 18.2 kohm.
  + Changes from LV2B to LV2C: Part number only, though this is a non-stock Digi-Key part, it should be easy to locate alternate sources, need new value for 5.0V sps rail.
* LV2C:GFE:R2255 [Capstone2006 designation: R255]
  + Part Description: 10.0 kohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant???, Rohm, MCR10EZHF1002 (Digi-Key p/n RHM10.0KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R255 along with R254 form a voltage divider with respect to the +3.3 V SPS output rail. When there is an overvoltage at the +3.3 V SPS output the voltage at the IN- pin (pin 4) of U2251 will be greater than the internal reference voltage of U2251 (typically 1.242 V) and will result in the comparator in U2251 outputting a logic high value. When the SPS output is below a certain threshold the input voltage (pin 4) to U2251 is less than the internal reference voltage and the comparator's output is a logic low.
  + Specifications/ Calculations: We specified R255 = 10.0 kohm. See R254.
  + Changes from LV2B to LV2C: Part number only, need to recalculate value for new SPS rail at 5.0V
* LV2C:GFE:C2206 [Capstone2006 designation: C203] Node Power Supply Filter Capacitor
  + Part Description: 22 uF, 25 V, Tant, T491 Series, 7343-31 (EIA), Cut Tape, RoHS Compliant???, Kemet, T491D226K025AT (Digi-Key p/n 399-3782-1-ND $0.65/1) http://www.kemet.com/kemet/web/homepage/kechome.nsf/vapubfiles/F3102T491.pdf/$file/F3102T491.pdf.
  + Purpose: C203 acts as a noise filter between the power bus and SPS. It also serves as a local energy storage node.
  + Specifications/ Calculations: It needs to have a voltage rating greater than 20 V and a low equivalent series resistance (ESR) thus a tantalum capacitor was chosen due to their low ESR at a higher capacitance.
  + Changes from LV2B to LV2C: Part number only. No recognized need for other changes, though the voltage rating is a bit low.
* LV2C:GFE:C2207 [Capstone2006 designation: C204]
  + Part Description: 0.33 uF, 50 V, 0805, X7R, Cut Tape, RoHS Compliant, Murata Electronics North America , GRM219R71H334KA88D (Digi-Key p/n 490-3327-1-ND $3.09/10) http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/GRM219R71H334KA88.pdf.
  + Purpose: C2207 is a high frequency noise filter between the power bus and SPS. It did not have to have as high a capacitance as C2206 so the trade off was to get a lower value at a low ESR.
  + Specifications/ Calculations: It needs to have a voltage rating greater than 20 V and the capacitance value was not very critical but should be much lower than C2206.
  + Changes from LV2B to LV2C: Part number only. No recognized need for other changes, though the voltage rating is a bit low.
* LV2C:GFE:C2250 [Capstone2006 designation: C250]
  + TLV3012AIDBVT "Secondary Power Supply" Cap (C2250)
  + Part Description: 2.7 uF, 10 V, 0805, X5R, Cut Tape, RoHS Compliant, Kemet, C0805C275K8PACTU (Digi-Key p/n 399-3127-1-ND $7.02/10) http://www.kemet.com/kemet/web/homepage/kechome.nsf/vapubfiles/F3102X5R.pdf/$file/F3102X5R.pdf.
  + Purpose: Along with CR2250, C2250 forms the power supply for U2251. C2250 is charged to a voltage less a forward diode drop (see CR2250) from the +3.3 V SPS output rail under normal operating conditions. U2251 draws a constant 2.8 uA supply current so CR2250 is always trickle charging C2250, therefore the voltage across C2250 will be VfCR2250 = 0.37 V (this is worst case Vf) less than 3.3 V. See CR2250. However U2251 can operate from 1.8 V to 5.0 V. Since the voltage at V+ of U2251 is approximately 3.0 V and the lower limit of the supply voltage range of U2251 is 1.8 V, C2250 has to be able to store enough charge such that if the SPS output drops down by a certain amount of voltage, U2251 is still powered for a certain amount of time thus preventing U2251 from power cycling if the SPS output ramps back up to +3.3 V. We want to prevent this because as U2251 is powering up the comparator could possibly switch. That behavior has to be observed in experiment but we assume that the initial state of the comparator will be logic low. If the SPS output toggles or drops in value we want U2251 to have power for a specified amount of time in case the magnitude of the voltage change of a transient causes a trigger event but lasts a very short amount of time or would normally shut down U2251, thus avoiding the time needed for U2251 to power cycle. When the overvoltage at the SPS output event occurs there is a finite amount of time required before Q2250 is eventually turned off namely the propagation delay of the comparator in U2251, the turn-on delay time of Q2251, the time to turn off Q2250 by U2250 and the turn-off delay time of Q2250. These typical times as are 12 us, 8 ns, 4 us and 26.2 ns as specified on pages 3, 3, 8 and 4 in the TLV3012, BSS1223, MAX5902 and ZXMP6A17E6 datasheets respectively, resulting in an ideal propagation delay of about 17 us. After these propagation delay times, Q2250 is off and the input voltage Vin (pin 2) of U200 is zero volts (after C201 is discharged) triggering the SHDN\ pin and turning off U200. When this happens the power supply to U2251 is essentially removed, so the time constant for C2250 has to be long enough such that as U2250 is going through its start sequence (150 ms) the comparator in U2251 can output a logic low and turn Q2251 off as the voltage it is comparing, IN+ (pin 3), to its internal reference voltage, REF, is the divided (see R254, R255) SPS output rail voltage which at this time is zero volts. To make sure that this sequence of events happen we specified U2251 to have power long enough to turn Q2251 back off while U2250 is turning back on again. Under normal operating conditions (no UVLO event) and assuming that there are no long or catastrophic transients, U2251 should always be on. This design will always keep U2250 on which will minimize any unknown states at the comparator output resulting from U2251 turning off, then on again, etc. Upon initial power up we assume that the output of U2251 will be logic low keeping Q2251 off to prevent a false overcurrent event for U2250 which may prevent the SPS from working as U2250 will never turn Q2250 on and will just cycle. This seems unlikely because upon initial power up, U2251 has no power and cannot output logic high. However as the +3.3 V SPS output is being brought up the output of the comparator is undefined which is not good being directly connected to the gate of Q2251 but we still think that Q2251 will remain off or will rapidly switch off if it is ever on after the transients.
  + Specifications/ Calculations: We calculated the needed amount of charge, Qt, C2250 would have to store such that U2251 would have power for at least 0.5 s (our specified amount of time U2251 should have power during these events) given that the SPS output voltage dropped by 1 V from which we calculated C2250's capacitance. C2250 = [((Qt \* 1.2) + (Iq \* tp))] / Vp, where Qt = [((Input Capacitance) \* Vt) + ((Reverse Transfer Capacitance) \* Vin)], Iq = 2.8 uA, ts = 0.5 s, Vp = 1 V Qt is the sum of products of the input capacitance of Q2251 times the maximum threshold voltage plus the reverse transfer capacitance of Q2251 times the maximum Vds swing, namely Vin. Iq is the supply current of U2251, tp is the amount of time we want U2251 to have power, Vp is the amount of voltage the SPS output drops and the 1.2 term is a fudge factor because Qt is dependent on some other factors not explicitly shown. tp was specified to be 0.5 s, this time is the time C2250 can supply power to U2251 which is longer than the propagation delays mentioned above including some margin just in case any trigger events do not go away and U2250 has to go through another 150 ms start sequence. If the trigger events remain longer than the 0.5 s, then U2251 turns off and the whole SPS will go through another initial power up sequence. Vp = 1 V, i.e. the input voltage V+ (pin 6) to U2251 can drop to about 3.0 V - 1 V = 2 V. Iq = 2.8 uA, see page 3 in the TLV3012 datasheet. Qt = (85 pF \* 2 V) + (15 pF \* 20V) = 470 pC, see page 3 in the BSS123 datasheet. C2250 = 1.40056 uF we decided to chose a 2.7 uF cap to give us a little more tp due to any unknown delays and the like we did not consider.
  + Changes from LV2B to LV2C: Part number only, still in stock at Digi-Key.
* LV2C:GFE:C2251 [Capstone2006 designation: C251]
  + TLV3012AIDBVT Overvoltage Detection Cap (C2251)
  + Part Description: 0.015 uF, 100 V, 0805, X7R, Cut Tape, RoHS Compliant, AVX Corporation, 08051C153KAT2A (Digi-Key p/n 478-1359-1-ND $2.64/10) http://rocky.Digi-Key.com/WebLib/AVX/Web%20Data/X7R%20(C).pdf.
  + Purpose: C2251 is used as a low-pass filter to node IN+ (pin 3) of U2251 and as positive feedback to make the comparator switch faster and to make sure that once the comparator is switching it completes the transition. Under normal SPS operation, when U2251 is keeping Q2251 off, the OUTPUT (pin 1) of U2251 is at zero volts thus the cap is acting like a low-pass filter, the node connected to pin 3 of U2251 is the input to the filter. If there are transients at the +3.3 V SPS output this node will also experience proportional transients. If the magnitude of these transients are great enough (but fast in duration) then U2251's comparator switches, which is undesirable so we want true ovevoltage events to trigger the comparator. C2251 will remove most of these false event transients. When there is a true overvoltage event the comparator starts to switch. If there is another transient (false event) where the magnitude of the voltage goes below the threshold the comparator could possibly try to switch back. We want the comparator to avoid reacting to false transients. C2251 prevents this because as the comparator is rising its output voltage, C2251 raises the voltage on pin 3 of U2251 thus reinforcing the comparator to keep on raising its output voltage. This is positive feedback. Also C2251 decreases the rise time of the comparator. Basically if there is something weird going on at the SPS output, i.e. it is oscillating between 0 V and 3.3 V, C2251 will help to make sure that U2251 turns Q2251 off, eventually turning off Q2250 which will give a 150 ms time period for the weird things to go away, given that U2251 does not shutdown during these transients. See C2250.
  + Specifications/ Calculations: We wanted C2251 to filter transients which lasted less than 100 us therefore we need to find the output resistance C2251 sees under a transient (or AC) condition. We used the zero-time coefficient technique to solve for the resistance and eventual capacitance. Under a transient condition the SPS output and comparator output are grounded (DC voltage) and removing C2251 the resistance it sees is the parallel combination of R254 and R255. R254 || R255 = 6.46 kohm, with an RC = 100 us we can solve for C = 15.4 nF. The closest standard value is 0.015 uF. The voltage rating needs to be greater than 20 V just for safe measure.
  + Changes from LV2B to LV2C: Part number only, still in stock at Digi-Key.
* LV2C:GFE:L2203 [Capstone2006 designation: L201] Power Bus input Choke
  + Part Description: CMS2-4-R Common Mode Inductors 102 uH, Micro-PAC Plus Package, RoHS Compliant, Cut Tape, (Digi-Key p/n: 513-1115-1-ND, $3.37/1). http://www.cooperet.com/library/products/PM-4313%20CMS-Series.pdf.
  + Purpose: Common mode choke (balanced inductor). It is used as an EMI filter between the power bus and the SPS.
  + Specifications/ Calculations: The capstone 2006 value was chosen through a trial and error process from the previous LV2 SPS design. Each inductor of the choke is 100 uH. See page 13 of the CAN Node Switch Mode Power Supply (SPS) (200) section in the Component Design for LV2 Power Electronics (Except Main Battery) engineering design notes
  + Changes from LV2B to LV2C: Capstone 2006 part (CMS1-11-R) has gone non-stock at Digi-Key and replacements are available in lots of 2000. New suggested part(CMS1-7-R) is dissimilar in value, but same physical size.

#### HAP Parts

* LV2C:GFE:U2203 TPS63000 Hap Output Regulator
  + The HAP output regulator IC (TI TPS63000) takes the voltage supplied by the battery or charger in the HAP and DC-DC converts it to the required voltages for the remainder of the circuit. In most cases this is 3.3V, though with small modifications this voltage can be set to anywhere from 2.5 to 5.5 Volts. C2221 is a simple bulk input capacitor and serves to filter transient spikes and noise from the input power. R2011 and C2222 act in concert to create a time constant that is used to ensure that power is ready to be supplied before the control circuit begins operation. L2202 is the Inductor used in the output filter of the Buck-Boost supply. R2216 and R2217 create a voltage divider that completes the feedback loop, R2216 is bypassed with capacitor C2223 to provide faster response to transient spikes. R2216 should be set for 1Mohm for operation of the circuit at 3.3Vdc or can be replaced by a 1.8Mohm resistor for the circuit to operate at 5Vdc, though Inductor L1 may need to be resized for this capability to be safely implemented. C2224 is used as the output filter capacitor and fulfills the role of reducing switch noise on the output. The circuit is synchronized to the 1.5MHz clock that is stepped down from the system clock by connection to the PS/Sync pin. This results in constant frequency operation that should not interfere in audio bands. The TPS63000 is noteworthy in that it acts as either a Buck regulator or a boost regulator and not as an inefficient buck-boost regulator. It manages this by only activating two of its four internal switches at a given time. The TPS63000 changes automatically from buck to boost operation as required on a per cycle basis.
* LV2C:GFE:U2204 LTC4085 HAP Battery Charger and Power Path Controller
  + The HAP battery charger is built around the LTC4085 battery charger IC from Linear Technologies. The LTC4085 is a linear charger that has the capability to control 2 external P-MOS devices while charging the battery. During normal operation power is supplied by the SPS (LV2C:GFE:U2202) and there is no need for the battery. While power is supplied from the SPS The !ACPR! signal from the charger (AC power Present, though in our case the power is DC) will enable power-flow through Q2204 to the HAP Output Regulator (LV2C:GFE:U2003) bypassing the LTC4085. During loss of SPS power, the !ACPR! signal goes away blocking the reverse flow of power from the battery toward the SPS. Anytime the load draws the output voltage down, the ideal diode controller in the LTC4085 will begin to feed power from the battery to the load. This is done both through an internal ideal diode between the BAT and OUT pins, as well as by controlling the gate of Q2205 and using it in parallel with the internal diode. Paralleling the internal diode allows lower resistance sourcing of the battery power to the load. The !CHRG! pin is ground3ed to indicate the battery is charging when the charge current threshold is passed. Threshold is at 5000V/Rprog, or 50mA.
* LV2C:GFE:D2202
  + Suggested Part: Digi-Key 475-1278-1-ND (OSRAM Semiconductor: LS R976-NR-1-0-20-R18), 0805 package, 2.0Vfwd, 20mA test = 104mcd
  + When the battery charge current is above 50mA this LED is lit indicating the battery is charging. The LED is chosen as a red LED since it will be indicating that battery is charging when it is lit. We don't want it to draw a lot of power, so it has been chosen as a 2mA part in an 0805 package. While not bright, it should be useable. The current is set by resistor R2213 to be 2mA when the battery is charging (Vout-Vfwd)/Iset = (4.2V-20V)/2mA = 1100 ohms.
* LV2C:GFE:B2201
  + Suggested Part:
* LV2C:GFE:R2207 Rprog
  + Suggested Part: Digi-Key (), 100k ohm, 0805 package.
  + The value of this resistor sets the charging current to the battery. The voltage across it can also be monitored by the LPC2348 to get an idea of the actual charge rate at any given moment. With Rprog = 100k ohms the charge current is set to 500mA. Ichrg(A)=50,000V/Rprog.
* LV2C:GFE:R2208 Rclprog
  + Suggested Part: Digi-Key (), 660 ohm, 0805 package.
  + The Current Limit Program resistor sets the input to output current limit. During normal operation and battery backup operation we will not be depending on the input to output current, as it is likely a higher voltage drop path than that of Q2204. It is currently set at 1.5A in case Q2204 is not populated on a given board, though that would also require pin 7 (wall) to be grounded. Icl(A)=1000V/Rclprog, Rclprog = 660 ohms for 1.515A max. Voltage on the Clprog pin is always proportional to the current flowing from In to Out and can be calculated by In(A)=(Vclprog/Rclprog)\*1000
* LV2C:GFE:R2209 Rnom
  + Suggested Part: Digi-Key (), 121k, 1%, 0805 package.
  + This resistor forms a voltage divider circuit with the thermistor R2214 and its delta modifying resistor R2215 which results in a voltage delivered to the NTC pin that represents the current temperature of the battery. As we want the thermistor to use a minimum amount of power in this design, we are using a 100k thermistor. The resistor value is then calculated by: Rnom=((Rcold-Rhot)/(2.815-.4086))\*Rntc (where Rntc is 100k @25C and Rcold is 3.363 @0C, Rhot is .3507 @50C (3.363 and .3507 are from the conversion table for the Vishay thermistor R2214 <<http://www.vishay.com/docs/33011/convtabs.pdf>>) resulting in a value of 125k, using the nearest standard 1% resistor results in Rnom = 121k ohms.
* LV2C:GFE:R2211
  + Suggested part: 100 Ohms
  + Value from Datasheet. In combination with C2222 this resistor creates a time constant that forces the controller to wait for power to be applied to the switches before the controller begins operation.
* LV2C:GFE:R2212 Gate Pull-Up
  + Suggested Part: Digi-Key (), 1k ohm, 0805package.
  + This resistor is used to pull the gate voltage up to the output voltage when the !ACPR! signal is not present.
* LV2C:GFE:R2213 Diode Current limit
  + Suggested Part: Digi-Key (), 1000 Ohms, 0805 package.
  + This resistor sets the current through diode D2202. Current flows when the LTC4085 pulls the !CHRG! pin low indicating that the battery is charging. (Vout-Vfwd)/Iset = (4.2V-2.0V)/2mA = 1100 ohms, use 1k as it is still close and should result in only a 2.2mA current draw during use.
* LV2C:GFE:R2214 Thermistor
  + Suggested Part: Digi-Key 541-1140-1-ND (Vishay/Dale NTHS0805N17N1003JE)
  + This thermistor is an 0805 package with a 100k ohm value at 25C. Rntc is 100k @25C and Rcold is 3.363 @0C, Rhot is 0.3507 @50C (3.363 and .3507 are from the conversion table for the Vishay thermistor R2214 <<http://www.vishay.com/docs/33011/convtabs.pdf>>)
* LV2C:GFE:R2215 R-delta
  + Suggested Part: Digi-Key (), 15k, 1%, 0805 package.
  + This resistor forms a voltage divider circuit with the thermistor R2214 and bias resistor R2209 which results in a voltage delivered to the NTC pin that represents the current temperature of the battery. This particular resistor is in series with the thermistor and widens the temperature delta of the thermistor to set 50C as the the T-hot trip point. The resistor value is calculated by: Rdelta=([(.04086/(2.815-.4086))*(Rcold-Rhot)]-Rhot)*Rntc (where Rntc is 100k @25C and Rcold is 3.363 @0C, Rhot is .3507 @50C (3.363 and .3507 are from the conversion table for the vishay thermistor R2214 <<http://www.vishay.com/docs/33011/convtabs.pdf>>) resulting in a value of 16k, using the nearest standard 1% resistor results in Rnom = 15k ohms.
* LV2C:GFE:R2216 Feedback Resistor
  + Suggested part: 1M ohm resistor for 3.3V operation.
  + R2216 calculation (3.3V): 1.12MOhm = R2*((Vout/Vfb)-1), Vout = 3.3V, Vfb = 500mV, R2217 = 200kohms*
  + *Suggested part: 1.8M ohms for 5V operation, ensure that L2202 is capable of safe operation at 5Vdc before making this change.*
  + *R2216 calculation (5V): 1.8MOhm = R2*((Vout/Vfb)-1), Vout = 5.0V, Vfb = 500mV, R2217 = 200kohms
* LV2C:GFE:R2217 Feedback Resistor
  + suggested part: 200k Ohms
  + datasheet recommends keeping this part in the range of 200k ohms. No good reason to change this, though the efficiency could be slightly better if a larger value is used. Keep Feedback divider current at or above 1uA.
* LV2C:GFE:C2219 Charge Timer Capacitor
  + Suggested Part: Digi-Key (),
  + This capacitor sets the duration of the Charge timer for the LTC4085. Ttimer(hours)=(Ctimer*Rprog*3hours)/(0.1uF\*100k)
* LV2C:GFE:C2220 Bulk Output capacitor
  + Suggested Part: Digi-Key (), 4.7uF
  + Datasheet recommends at least 4.7uF bypass cap from the OUT pin of the LTC4085 to ground. This capacitor holds up the output voltage when the battery is initially switched in, a job that could possibly be handled by C2221 if it is close enough to the switches.
* LV2C:GFE:C2221 Bulk Input Capacitor
  + Suggested part: 4.7uF, X7R ceramic
  + Value is as suggested in Datasheet, recommend small ceramic cap as close to pins as possible.
* LV2C:GFE:C2222
  + Suggested part: 0.1uF, X7R ceramic
  + Value from datasheet. In combination with R2211 this capacitor creates a time constant that forces the controller to wait for power to be applied to the switches before the controller begins operation.
* LV2C:GFE:C2223 FeedForward Capacitor.
  + Suggested part (3.3V): 2pF, X7R ceramic
  + C2223(3.3V)= 1.96pF = Feedforward capacitor = 2.2uS/R1
  + Suggested part (5.0V): 1.2pF, X7R ceramic
  + C2223(5V)= 1.22pF = Feedforward capacitor = 2.2uS/R1
* LV2C:GFE:C2224 Bulk Output Capacitor
  + Suggested part: 22uF, X7R ceramic
  + C2224(min) = 11uF = Cout=5*L*(uF/uH), L=2.2uH. In combination with L2202, this capacitor acts as the output filter, datasheet recommends small ceramic cap as close to Vout and Pgnd pins as possible.
* LV2C:GFE:L2202 Filter Inductor
  + Suggested Part: Digi-Key 587-1669-1-ND (Taiyo Yuden NR4018T2R2M), 2.2uH surface mount power inductor.
  + Recommended value: 2.2uH, 1.75A Irms, 2.26A Isat
  + L2202(suggested) = 2.2uH, this is the inductor value suggested in the datasheet for 3.3V operation.
  + L2202(min) = 1.57uH, this is the larger of 1.57uH = (Vout*(Vinmax-Vout)/(Vinmax*f*0.3A) or 1.34uH = (Vin\_min*(Vout-Vin*min))/(Vin*min*f*0.3A), where Vout=3.3V, Vin*min=2.5V, Vin*max=4.2V, f=1.5MHz.
  + Imax(3.3V) = 1.74A, Isat= 2.26A = Imax+30%
* **HAP Legacy devices:** This category includes much of the front-end protection circuitry (Capstone 2006 Frontend Passive Block) and includes devices that have carried over from the 2006 capstone design, often with few or no changes.
* LV2C:GFE:D2203 [Capstone2006 designation: D201] SPS Output Power On LED
  + Part Description: 1.9 V, 90 mcd @ 20 mA, 609 nm, 0805, Orange Diffused LED, CML Innovative Technologies Inc, CMDA5BA7D1S (Digi-Key p/n L71515CT-ND $3.00/10) http://www.chml.com/pdf/temp/CMDA5BA7D1S.pdf.
  + Purpose: This is an orange LED which is lit given that the nominal SPS 3.3 V rail is up. It is mainly used as an initial indicator of the 3.3 V rail's status. Orange was an arbitrary choice, however any other LEDs in the Glue Logic section needed to be different colors. The intensity and viewing angle are not critical since the only time the information from the LED is useful is in trouble shooting on the ground. It remains lit throughout the whole flight.
  + Specifications/ Calculations: From the CMDA5BA7D1S datasheet, Vf = 1.9 V. We specified the LED drive current to be 2 mA. See R2241 for I-V calculations.
  + Changes from LV2B to LV2C: Part number only.
* LV2C:GFE:CR2201 [Capstone2006 designation: CR251] SPS Secondary Buck (Catch) Schottky Diode
  + Part Description: 30 V, 1.5 A, 4 ns, New MiniPower 2P, Cut Tape, RoHS Compliant???, Panasonic - SSG, MA2Q70500L (Digi-Key p/n MA2Q70500LCT-ND $0.83/1) http://www.semicon.panasonic.co.jp/ds/eng/SKH00017BED.pdf.
  + Purpose: CR2201 along with C2252 and L2202 form the second buck switching voltage power regulator which will be eventually regulated down to 5 V possibly with a low-dropout (LDO) linear voltage regulator. For consistency we used the same Schottky diode as CR200. Also the general understanding was that this secondary buck will power specific parts like 5 V ADCs on certain nodes (like the IMU) and we expect that this diode's rated specs are more than enough.
  + Specifications/ Calculations: Using the formula on page 9 in the LT1767 datasheet we calculated the average DC current that CR251 should be able to handle. Id,avg = Io (Vin - Vout) / Vin, where Io is the secondary output current of the SPS, Vin is the voltage at the node which is between L200a and L200b and Vout is the SPS secondary output voltage. We assumed that Vin would be switching somewhere between 1.6 V and 7 V. With Vout = 5 V and using the worst case Io = 1 A and Vin = 7 V values Id,avg = 286 mA (again this diode is overrated). We knew that not every node would need a secondary 5 V supply but even the ones that did, the added current should not cause overcurrent events (see U2250). Hopefully.
  + Changes from LV2B to LV2C: Part number only. Due to the nature of the new TPS63000, this is unlikely to function. In LV2B this was connected to a simple buck supply and could have worked. In LV2C, it is unlikely to raise the voltage from 3.3 to 5 volts, but it has been left in as it can be depopulated if it turns out to be nonfunctional.
* LV2C:GFE:R2241 [Capstone2006 designation: R214 or R241] 3.3V Output Power On LED Current Limiter Resistor
  + Part Description: 649 ohm, 0805, 1%, 1/8 W, Cut Tape, RoHS Compliant, Rohm, MCR10EZHF6490 (Digi-Key p/n RHM649CCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
  + Purpose: R2241 is the SPS Output Power On LED current limiting resistor.
  + Specifications/ Calculations: From the datasheet Vf = 1.9 V, resulting in a current limiting resistor of about, R2241 = (3.3 V - 1.9 V) / (2 mA) = 650 ohms. The closest standard value was 649 ohms.
  + Changes from LV2B to LV2C: Part number only.
* LV2C:GFE:C2252 [Capstone2006 designation: C252]
  + Part Description: TBD
  + Purpose: This cap along with C2252A, CR2251 and L2202 form the second buck switching voltage power supply which will be eventually regulated down to 5 V possibly with a low-dropout (LDO) linear voltage regulator. These are application specific caps whose values are mostly independent from the SPS design.
  + Specifications/ Calculations: The only difference between C2252 and C2252a are the packages and that only one of them will actually be on the PCB. Since we do not know any details about the actual application specific circuitry each SPS will power from an SPS design point of view, we chose to use both a 0805 and 1206 package. We chose two packages because we moved all relevant parts to the 0805 package from 1206 as in the LV2 SPS design and in case a specific application node needs a more beefy cap a 1206 package cap can be used. The layout of the parts will not be side by side as suggested in the schematic but are offset and superimposed on top of each other on the same side of the PCB. Because only one cap will be used we offset the pads such that they are not directly on top of each other and either package can be placed down thus saving space. The values are TBD.
  + Changes from LV2B to LV2C: Part number only. Due to the nature of the new TPS63000, this is unlikely to function. In LV2B this was connected to a simple buck supply and could have worked. In LV2C, it is unlikely to raise the voltage from 3.3 to 5 volts, but it has been left in as it can be depopulated if it turns out to be nonfunctional.
* LV2C:GFE:C2252A [Capstone2006 designation: C252A]
  + Part Description: TBD
  + Purpose: This cap along with C2252, CR2251 and L2202 form the second buck switching voltage power supply which will be eventually regulated down to 5 V possibly with a low-dropout (LDO) linear voltage regulator. These are application specific caps whose values are mostly independent from the SPS design.
  + Specifications/ Calculations: The only difference between C2252 and C2252a are the packages and that only one of them will actually be on the PCB. Since we do not know any details about the actual application specific circuitry each SPS will power from an SPS design point of view, we chose to use both a 0805 and 1206 package. We chose two packages because we moved all relevant parts to the 0805 package from 1206 as in the LV2 SPS design and in case a specific application node needs a more beefy cap a 1206 package cap can be used. The layout of the parts will not be side by side as suggested in the schematic but are offset and superimposed on top of each other on the same side of the PCB. Because only one cap will be used we offset the pads such that they are not directly on top of each other and either package can be placed down thus saving space. The values are TBD.
  + Changes from LV2B to LV2C: Part number only. Due to the nature of the new TPS63000, this is unlikely to function. In LV2B this was connected to a simple buck supply and could have worked. In LV2C, it is unlikely to raise the voltage from 3.3 to 5 volts, but it has been left in as it can be depopulated if it turns out to be nonfunctional.

#### Microcontroller Pin Tables

The microcontroller pin tables contain a listing of signal versus pin number in the first table, and a listing of pin number, signal name, signal destination, and whether or not a pin is used by the GFE. Pins that are in use by the GFE are not available for use by Node Specific Hardware without careful consideration of the impact to the GFE functionality.

|  |  |  |
| --- | --- | --- |
|  | Sort by Signal | |
| Pin | **Signal** |  |
| 46 | PORT0.0/RD1/TXD3/SDA1 | |
| 47 | PORT0.1/TD1/RXD3/SCL1 | |
| 98 | PORT0.2/TXD0 | |
| 99 | PORT0.3/RXD0 | |
| 81 | PORT0.4/I2SRX\_CLK/RD2/CAP2.0 | |
| 80 | PORT0.5/I2SRX\_WS/TD2/CAP2.1 | |
| 79 | PORT0.6/I2SRX\_SDA/SSEL1/MAT2.0 | |
| 78 | PORT0.7/I2STX\_CLK/SCK1/MAT2.1 | |
| 77 | PORT0.8/I2STX\_WS/MISO1/MAT2.2 | |
| 76 | PORT0.9/I2STX\_SDA/MOSI1/MAT2.3 | |
| 48 | PORT0.10/TXD2/SDA2/MAT3.0 | |
| 49 | PORT0.11/RXD2/SCL2/MAT3.1 | |
| 62 | PORT0.15/TXD1/SCK0/SCK | |
| 63 | PORT0.16/RXD1/SSEL0/SSEL | |
| 61 | PORT0.17/CTS1/MISO0/MISO | |
| 60 | PORT0.18/DCD1/MOSI0/MOSI | |
| 59 | PORT0.19/DSR1/MCICLK/SDA1 | |
| 58 | PORT0.20/DTR1/MCICMD/SCL1 | |
| 57 | PORT0.21/RI1/MCIPWR/RD1 | |
| 56 | PORT0.22/RTS1/MCIDAT0/TD1 | |
| 9 | PORT0.23/AD0.0/I2SRX\_CLK/CAP3.0 | |
| 8 | PORT0.24/AD0.1/I2SRX\_WS/CAP3.1 | |
| 7 | PORT0.25/AD0.2/I2SRX\_SDA/TXD3 | |
| 6 | PORT0.26/AD0.3/AOUT/RXD3 | |
| 25 | PORT0.27/SDA0 | |
| 24 | PORT0.28/SCL0 | |
| 29 | PORT0.29/USB\_D+ | |
| 30 | PORT0.30/USB\_D- | |
| 95 | PORT1.0/ENET\_TXD0 | |
| 94 | PORT1.1/ENET\_TXD1 | |
| 93 | PORT1.4/ENET\_TX\_EN | |
| 92 | PORT1.8/ENET\_CRS | |
| 91 | PORT1.9/ENET\_RXD0 | |
| 90 | PORT1.10/ENET\_RXD1 | |
| 89 | PORT1.14/ENET\_RX\_ER | |
| 88 | PORT1.15/ENET\_REF\_CLK | |
| 87 | PORT1.16/ENET\_MDC | |
| 86 | PORT1.17/ENET\_MDIO | |
| 32 | PORT1.18/USB\_UP\_LED/PWM1.1/CAP1.0 | |
| 33 | PORT1.19/CAP1.1 | |
| 34 | PORT1.20/PWM1.2/SCK0 | |
| 35 | PORT1.21/PWM1.3/SSEL0 | |
| 36 | PORT1.22/MAT1.0 | |
| 37 | PORT1.23/PWM1.4/MISO0 | |
| 38 | PORT1.24/PWM1.5/MOSI0 | |
| 39 | PORT1.25/MAT1.1 | |
| 40 | PORT1.26/PWM1.6/CAP0.0 | |
| 43 | PORT1.27/CAP0.1 | |
| 44 | PORT1.28/PCAP1.0/MAT0.0 | |
| 45 | PORT1.29/PCAP1.1/MAT0.1 | |
| 21 | PORT1.30/VBUS/AD0.4 | |
| 20 | PORT1.31/SCK1/AD0.5 | |
| 75 | PORT2.0/PWM1.1/TXD1/TRACECLK | |
| 74 | PORT2.1/PWM1.2/RXD1/PIPESTAT0 | |
| 53 | PORT2.10/!EINT0 | |
| 52 | PORT2.11/!EINT1/MCIDAT1/I2STX\_CLK | |
| 51 | PORT2.12/!EINT2/MCIDAT2/I2STX\_WS | |
| 50 | PORT2.13/!EINT3/MCIDAT3/I2STX\_SDA | |
| 73 | PORT2.2/PWM1.3/CTS1/PIPESTAT1 | |
| 70 | PORT2.3/PWM1.4/DCD1/PIPESTAT2 | |
| 69 | PORT2.4/PWM1.5/DSR1/TRACESYNC | |
| 68 | PORT2.5/PWM1.6/DTR1/TRACEPKT0 | |
| 67 | PORT2.6/PCAP1.0/RI1/TRACEPKT1 | |
| 66 | PORT2.7/RD2/RTS1/TRACEPKT2 | |
| 65 | PORT2.8/TD2/TXD2/TRACEPKT3 | |
| 64 | PORT2.9/USB\_CONNECT/RXD2/EXTIN0 | |
| 27 | PORT3.25/MAT0.0/PWM1.2 | |
| 26 | PORT3.26/MAT0.1/RXD3 | |
| 82 | PORT4.28/MAT2.0/TXD3 | |
| 85 | PORT4.29/MAT2.1/RXD3 | |
| 17 | !RESET |  |
| 14 | !RSTOUT |  |
| 100 | RTCK |  |
| 16 | RTCX1 |  |
| 18 | RTCX2 |  |
| 5 | TCK |  |
| 2 | TDI |  |
| 1 | TDO |  |
| 3 | TMS |  |
| 4 | !TRST |  |
| 19 | VBAT |  |
| 28 | VDD(3V3) | |
| 54 | VDD(3V3)@1 | |
| 71 | VDD(3V3)@2 | |
| 96 | VDD(3V3)@3 | |
| 13 | VDD(DCDC)(3V3) | |
| 42 | VDD(DCDC)(3V3)@1 | |
| 84 | VDD(DCDC)(3V3)@2 | |
| 10 | VDDA |  |
| 12 | VREF |  |
| 15 | VSS |  |
| 31 | VSS@1 |  |
| 41 | VSS@2 |  |
| 55 | VSS@3 |  |
| 72 | VSS@4 |  |
| 97 | VSS@5 |  |
| 83 | VSS@6 |  |
| 11 | VSSA |  |
| 22 | XTAL1 |  |
| 23 | XTAL2 |  |

|  |  |  |  |
| --- | --- | --- | --- |
|  | Sort by Pin and Purpose (Generic Node Only) | | |
| Pin | **LPC2368 Signal Name** | **Destination** | **Available** |
| 1 | TDO | Debug-P7 | no |
| 2 | TDI | Debug-P6 | no |
| 3 | TMS | Debug-P8 | no |
| 4 | !TRST | Debug-P9 | no |
| 5 | TCK | Debug-P5 | no |
| 6 | PORT0.26/AD0.3/AOUT/RXD3 | No-connect | yes |
| 7 | PORT0.25/AD0.2/I2SRX\_SDA/TXD3 | No-connect | yes |
| 8 | PORT0.24/AD0.1/I2SRX\_WS/CAP3.1 | No-connect | yes |
| 9 | PORT0.23/AD0.0/I2SRX\_CLK/CAP3.0 | No-connect | yes |
| 10 | VDDA | A\_3P3 | no |
| 11 | VSSA | A\_GND | no |
| 12 | VREF | CPU\_VREF | no |
| 13 | VDD(DCDC)(3V3) | 3.3V\_HAP\_OUT | no |
| 14 | !RSTOUT | Debug-P3 | no |
| 15 | VSS | GND | no |
| 16 | RTCX1 | RTC\_XTAL-A | no |
| 17 | !RESET | Debug-P2 | no |
| 18 | RTCX2 | RTC\_XTAL-B | no |
| 19 | VBAT | CPU\_VBAT | no |
| 20 | PORT1.31/SCK1/AD0.5 | BAT\_CHRG\_MONITOR | no |
| 21 | PORT1.30/VBUS/AD0.4 | No-connect | yes |
| 22 | XTAL1 | CPU\_XTAL1 | no |
| 23 | XTAL2 | CPU\_XTAL2 | no |
| 24 | PORT0.28/SCL0 | No-connect | yes |
| 25 | PORT0.27/SDA0 | No-connect | yes |
| 26 | PORT3.26/MAT0.1/RXD3 | No-connect | yes |
| 27 | PORT3.25/MAT0.0/PWM1.2 | No-connect | yes |
| 28 | VDD(3V3) | 3.3V\_HAP\_OUT | no |
| 29 | PORT0.29/USB\_D+ | USB\_D+ | no |
| 30 | PORT0.30/USB\_D- | USB\_D- | no |
| 31 | VSS@1 | GND | no |
| 32 | PORT1.18/USB\_UP\_LED/PWM1.1/CAP1.0 | GPIO\_USB\_HighSpeed | no |
| 33 | PORT1.19/CAP1.1 | No-connect | yes |
| 34 | PORT1.20/PWM1.2/SCK0 | No-connect | yes |
| 35 | PORT1.21/PWM1.3/SSEL0 | No-connect | yes |
| 36 | PORT1.22/MAT1.0 | No-connect | yes |
| 37 | PORT1.23/PWM1.4/MISO0 | No-connect | yes |
| 38 | PORT1.24/PWM1.5/MOSI0 | No-connect | yes |
| 39 | PORT1.25/MAT1.1 | No-connect | yes |
| 40 | PORT1.26/PWM1.6/CAP0.0 | No-connect | yes |
| 41 | VSS@2 | GND | no |
| 42 | VDD(DCDC)(3V3)@1 | 3.3V\_HAP\_OUT | no |
| 43 | PORT1.27/CAP0.1 | No-connect | yes |
| 44 | PORT1.28/PCAP1.0/MAT0.0 | No-connect | yes |
| 45 | PORT1.29/PCAP1.1/MAT0.1 | No-connect | yes |
| 46 | PORT0.0/RD1/TXD3/SDA1 | CAN | no |
| 47 | PORT0.1/TD1/RXD3/SCL1 | CAN | no |
| 48 | PORT0.10/TXD2/SDA2/MAT3.0 | No-connect | yes |
| 49 | PORT0.11/RXD2/SCL2/MAT3.1 | No-connect | yes |
| 50 | PORT2.13/!EINT3/MCIDAT3/I2STX\_SDA | No-connect | yes |
| 51 | PORT2.12/!EINT2/MCIDAT2/I2STX\_WS | No-connect | yes |
| 52 | PORT2.11/!EINT1/MCIDAT1/I2STX\_CLK | No-connect | yes |
| 53 | PORT2.10/!EINT0 | Debug-P10 | no |
| 54 | VDD(3V3)@1 | 3.3V\_HAP\_OUT | no |
| 55 | VSS@3 | GND | no |
| 56 | PORT0.22/RTS1/MCIDAT0/TD1 | No-connect | yes |
| 57 | PORT0.21/RI1/MCIPWR/RD1 | No-connect | yes |
| 58 | PORT0.20/DTR1/MCICMD/SCL1 | No-connect | yes |
| 59 | PORT0.19/DSR1/MCICLK/SDA1 | No-connect | yes |
| 60 | PORT0.18/DCD1/MOSI0/MOSI | No-connect | yes |
| 61 | PORT0.17/CTS1/MISO0/MISO | No-connect | yes |
| 62 | PORT0.15/TXD1/SCK0/SCK | No-connect | yes |
| 63 | PORT0.16/RXD1/SSEL0/SSEL | No-connect | yes |
| 64 | PORT2.9/USB\_CONNECT/RXD2/EXTIN0 | No-connect | yes |
| 65 | PORT2.8/TD2/TXD2/TRACEPKT3 | No-connect | yes |
| 66 | PORT2.7/RD2/RTS1/TRACEPKT2 | No-connect | yes |
| 67 | PORT2.6/PCAP1.0/RI1/TRACEPKT1 | No-connect | yes |
| 68 | PORT2.5/PWM1.6/DTR1/TRACEPKT0 | No-connect | yes |
| 69 | PORT2.4/PWM1.5/DSR1/TRACESYNC | No-connect | yes |
| 70 | PORT2.3/PWM1.4/DCD1/PIPESTAT2 | No-connect | yes |
| 71 | VDD(3V3)@2 | 3.3V\_HAP\_OUT | no |
| 72 | VSS@4 | GND | no |
| 73 | PORT2.2/PWM1.3/CTS1/PIPESTAT1 | No-connect | yes |
| 74 | PORT2.1/PWM1.2/RXD1/PIPESTAT0 | No-connect | yes |
| 75 | PORT2.0/PWM1.1/TXD1/TRACECLK | No-connect | yes |
| 76 | PORT0.9/I2STX\_SDA/MOSI1/MAT2.3 | No-connect | yes |
| 77 | PORT0.8/I2STX\_WS/MISO1/MAT2.2 | No-connect | yes |
| 78 | PORT0.7/I2STX\_CLK/SCK1/MAT2.1 | No-connect | yes |
| 79 | PORT0.6/I2SRX\_SDA/SSEL1/MAT2.0 | No-connect | yes |
| 80 | PORT0.5/I2SRX\_WS/TD2/CAP2.1 | No-connect | yes |
| 81 | PORT0.4/I2SRX\_CLK/RD2/CAP2.0 | CAN\_Autobaud | no |
| 82 | PORT4.28/MAT2.0/TXD3 | No-connect | yes |
| 83 | VSS@6 | GND | no |
| 84 | VDD(DCDC)(3V3)@2 | 3.3V\_HAP\_OUT | no |
| 85 | PORT4.29/MAT2.1/RXD3 | No-connect | yes |
| 86 | PORT1.17/ENET\_MDIO | Status\_LED\_2 | no |
| 87 | PORT1.16/ENET\_MDC | Status\_LED\_1 | no |
| 88 | PORT1.15/ENET\_REF\_CLK | No-connect | yes |
| 89 | PORT1.14/ENET\_RX\_ER | GPIO\_HAP\_DISABLE | no |
| 90 | PORT1.10/ENET\_RXD1 | GPIO\_BAT\_!CHRG! | no |
| 91 | PORT1.9/ENET\_RXD0 | GPIO\_CHRGR\_DIS\_B | no |
| 92 | PORT1.8/ENET\_CRS | GPIO\_CHRGR\_DIS\_A | no |
| 93 | PORT1.4/ENET\_TX\_EN | GPIO\_SPS\_5V\_GOOD | no |
| 94 | PORT1.1/ENET\_TXD1 | GPIO\_SPS\_V-IN\_GOOD | no |
| 95 | PORT1.0/ENET\_TXD0 | GPIO\_SPS\_DISABLE | no |
| 96 | VDD(3V3)@3 | 3.3V\_HAP\_OUT | no |
| 97 | VSS@5 | GND | no |
| 98 | PORT0.2/TXD0 | Debug-P11 | no |
| 99 | PORT0.3/RXD0 | Debug-P12 | no |
| 100 | RTCK | Debug-P4 | no |

### Appendix B: APS Power Switch Parts Selection and Description

#### Integrated Circuits:

**U2000 - U2007**

* Texas Instruments TPS2490 Positive High-Voltage Power-Limiting Hotswap Controller
* This IC acts as the controller which determines whether or not the external FET is on/off based on several parameters. See above for in depth description of IC functions

#### Transistors:

**Q2000 - Q2007**

* Vishay Si4122DY N-Channel MOSFET
* These transistors are used in conjunction with the TPS2490 as described above

#### Connectors:

**J2000 - J2007**

* Modified JST-16PS-JED 16-pin Connector.
* These connectors are used to connect the 7 downstream devices and Flight-Computer to the power switches. The connectors are modified in that they have added "blocks" which allow the plugs from the external devices to be screwed into place, similar to the connection between monitor and computer of a desktop unit
* The pins of each connector are doubled up for redundancy and pin descriptions for each connector are as follows:
  + 2 pins - positive battery power/shore power, connected to the output of the FET on each switch
  + 2 pins - battery ground/shore ground
  + 2 pins - CAN-H; high level of differential CAN data signal
  + 2 pins - CAN-L; low level of differential CAN data signal
  + 2 pins - USB-H; high level of differential USB data signal
  + 2 pins - USB-L; low level of differential USB data signal
  + 2 pins - AUX-1; available for optional board to board connections
  + 2 pins - AUX-2; available for optional board to board connections

#### LEDs:

**LED2000 - LED2007**

* Green LEDs, 0805 package, used to indicate on/off state of the power switches

#### Resistors:

**R2000 - R2007**

* These resistors are the sense resistors (Rs as referred to in datasheet) used to set the current limit, Ilim, allowed through the FET
* VCC and SENSE pins are connected to the terminals of these resistors and the TPS2490 computes the voltage VCC - VSENSE. This voltage drop is compared internally to a 50mV threshold voltage via an internal comparator. If the voltage exceeds the 50mV threshold, an overcurrent condition exists and the TPS2490 begins limiting action.
* The value of these resistors is calculated as follows:

**R = 0.05V/(1.2 x Ilim)**

Where the factor of 1.2 ensures a 20% operating current tolerance

* With Ilim = 5A:

**R = 0.05V/(1.2 x 5) = 8.33mOhm**

**R2008 - R2015**

* Gate resistors used to minimize noise on the gate drive of each switch
* It is recommended in the TPS2490 datasheet that if Ciss of the MOSFET > 200pF, a 10 Ohm resistor should be used, otherwise this should be 33Ohm
* Ciss of the Si4122DY = 4200pF so these resistors will be 10 Ohm

**R2016 - R2023**

* The top resistor in the resistor divider circuit used in conjunction with the 4V reference voltage at VREF to set the voltage on the PROG pin and thus program the power limit for the constant power engine.
* Datasheet notes this resistor can be 4kOhm or greater but it is recommended that 10kOhm or greater be used so these resistors will be 10kOhm

**R2024 - R2031**

* The bottom resistor for the voltage divider circuit used in conjunction with the 4V reference voltage ate VREF to set the voltage on the PROG pin and program the power limit for the constant power engine
* With the power limit, Plim, already calculated to be 1.755W (see constant power limit engine description) the voltage needed at PROG pin can be calculated:

**Vprog = Plim/(10 x Ilim,max) = 1.755/(10 x (1.2x5)) = 0.02925V**

* With the top resistor value set at 10kOhm, the value of these resistors can be calculated by solving the following equation for R:

**Vprog = Vref(R/(10k + R))**

* Solving for R we obtain:

**R = 73.664Ohm**

* If we set these resistors at 75Ohm, Vprog becomes 0.02977V making Plim 1.79W which is an increase of only about 0.04W and doesn't seem as though it would present a problem

**R2032 - R2039**

* 10kOhm pull down resistors for the logic enable function of TPS2490
* In the event that the micro-controller malfunctions or for some reason does not turn on the TPS2490, this pull down ensures that the switch will be latched off

**R2040 - R2047**

* 10kOhm pull-up resistors for the power good (PG) pin.
* Since PG is open - drain when 'true', the pull-up ensures that PG goes high after Vds falls below 1.25V and a 9ms deglitch time has elapsed

**R2048 - R2055**

* These resistors are place holders in case the dV/dt control function is needed. At this point they are not placed

**R2056 - R2063**

* These resistors are current limit resistors to ensure LEDs don't burn up during operation.
* 5kOhm seems to be a reasonable value

#### Capacitors:

**C2000 - C2007**

* Timeout capacitors connected to the TIMER pin of the TPS2490 (Ct in the datasheet)
* These capacitors control the amount of time a fault is allowed before latch off
* The spec calls for a 100ms time delay
* It is given that during a fault, this capacitor is charged to 4V with a 25uA current before latch-off occurs, thus we can solve for the capacitor values as follows:

**I = C(dV/dt)**

* Where:

**I = 25uA**

**dV/dt = 4V/100ms**

* Thus:

**C = I/(dV/dt) = 25uA/(4V/100ms) = 0.625uF**

**C2008 - C2015**

* These capacitors are placeholders in case the soft start function is required (see function descriptions above)
* In this design, soft-start is not used so these capacitors are not placed

**C2016 - C2023**

* These capacitors are placeholders in the case that the optional dV/dt function is needed (see function description above)
* In this design we are not using the dV/dt function so these capacitors are not placed

**C2024 - C2031**

* 0.1uF bypass capacitors which act to eliminate high frequency glitches on VCC pin of TPS2490

**C2032, C2033**

* 0.1uF bypass capacitors to eliminate high frequency glitches between main power and main ground

**C2044 - C2051**

* 0.1uF ESD protection capacitors for the 16 pin connectors

### Appendix C: APS Umbilical Parts Selection and Description

#### Integrated Circuits:

**U2101**

* Ideal diode controller. See above for functionality

#### Transistors:

**Q2104**

* Functions as the ideal diode. See above for functionality

#### Resistors:

**R2119**

* 10kOhm Pull down for launch detect

#### Capacitors:

**C2107**

* 39uF bypass capacitor. This value is recommended in the datasheet

**C2108, C2109**

* 100nF bypass capacitors

#### Connectors:

**J21??**

* Shore power connector. Will be updated when Dave has an actual connector. As it stands now this is just an arbitrary 5-pin connector with the following connections:
  + RCKT\_RDY
    - Connects to the ARM which provides the flight computer with the signal indicating the rocket is ready for launch
  + SH\_TX
    - Transmit signal from shore power, this signal will connect to RX of the ARM. In the event of launch, the shore power umbilical will pull out of the connector and this signal will be pulled low by R2119 indicating to the ARM that launch has occurred.
  + SH\_RX
    - Receive signal to shore power, connects to TX of ARM
  + SH\_GND
    - Shore power ground
  + SH\_POWER
    - Main power from umbilical

### Appendix D: APS USB Hub Parts Selection and Description

#### Integrated Circuits:

**U2008**

* SMSC\_USB2517 USB hub chip
* See above for explanations

#### Resistors:

**R2064**

* 1MOhm filter resistor for external clock
* This resistor was included in the circuit based on the smsc reference design. Not sure if this is needed

**R2065**

* 12kOhm bias resistor sets the internal bias of the hub chip
* 2517 datasheet specifies this value of resistor on RBIAS pin
* See RBIAS pin description for more information

**R2066**

* 10kOhm pull-up resistor connected to the RESET-N pin
* This pull-up to 3.3V ensures the USB hub reset function is negated unless asserted by the ARM

**R2067-R2069**

* 10kOhm pulldown resistors for CFG-SEL[2:0] pins
* This ensures that the default configuration scheme of the usb hub will be CFG-SEL[2:0] = '000'
* See CFG-SEL[2] pin description for explanation of settings associated with this configuration
* These pins are also connected to GPIO pins of the ARM so that the HUB can be re-configured by the micro-controller if so desired

**R2070, R2071**

* These resistors are attached to multifunctional pins on the hub
* R2070 is a 10kOhm pull-down resistor ensuring that NON-REM[1] has a default logic low level (We are not using the other functions associated with this pin. This pin is also connected to a GPIO of the ARM so that other options can be used if needed
* R2071 is a 10kOhm pull-up resistor to ensure that SUSP-IND/LOCAL-PWR/NON-REM[0] pin has a default logic high level
  + In the event that the HUB is reset, this pin will generally need to be driven low by the ARM along with NON\_REM[1] to ensure that all 7 of the HUB's downstream ports are configured to support removable devices. This configuration can be changed if need be as both pins are connected to GPIO pins of the ARM
  + The pull-up is necessary because of the fact that a logic high is needed on this pin to tell the HUB that a local power source is present. If this is not a logic high, the HUB will think that all power is provided from the VBUS which we do not implement
  + If the ARM should fail to drive this pin low upon a reset, port 1 will be considered a non-removable port. This should not pose too much of a problem as the hub can be re-configured at any time.

**R2072, R2073**

* 10kOhm pull-down resistors connected to the BOOST[1:0] pins
* The pull-downs ensure that the default setting of the HUB's signal strength for downstream ports will be 'no-boost'
* These pins also connect to GPIO pins of the ARM so that the HUB can be reconfigured for signal boost if needed
* See BOOST[1:0] pin descriptions for more information

**R2074-R2080**

* 330 Ohm current limiting resistors to protect the LED port status indicators
* This value is questionable as the design uses 0605 LEDs and I'm not sure if such a small resistor provides enough protection.

#### Capacitors:

**C2034,C2035**

* 33pF bypass capacitors connected to the terminals of the external 24MHz clock
* These values were chosen based on the 2517 datasheet reference design

**C2036**

* 1uF capacitor connected from PLLFILT pin to ground, acts as a filter capacitor for the HUB's internal PLL
* This capacitor value is specified in the datasheet

**C2037**

* 0.1uF VDD core regulator filter capacitor, connects from CRFILT pin to ground
* This value is specified in the 2517 datasheet

**C2038-C2044**

* 0.1uF bypass capacitors to filter high frequency noise on the 7 VDD pins

#### LEDs:

**LED2008-LED2014**

* Green LED status indicators indicating the status of the 7 downstream ports
* These indicators provide downstream port connection status and work in conjunction with red LEDs (LED2015-LED2021) to indicate connection speed
* See LED2015-LED2021 description for more information about connection speed indication, also see section 6.1 in 2517 datasheet for detailed description of LED functionality
* The green status LEDs function in accordance with section 11.5.3 of USB 2.0 specification

**LED2015-LED2021**

* Red LEDs which work in conjunction with green LEDs (LED2008-LED2014) to indicate speed of the devices attached to the 7 downstream ports
* These and the green LEDs are connected to the LED-A-N[7:1] pins in such a way that they function as follows:
  + When any of the pins is driven to a logic low, the corresponding green LED will light up which indicates that a lowspeed device is attached to the respective port
  + When any of the pins is driven to a logic high, the corresponding red LED will light up indicating that a full speed device is attached to the respective port
  + When any of the pins outputs a 1kHz square wave, both LEDs will be pulsed on and off. The datasheet notes that the green/red LEDs should be in a single package so that this condition will result in an orange color, however we are using separate 0605 LEDs so it will simply appear as both the red and green LEDs are on. This indicates that a high speed device is attached to the respective downstream port
  + When nothing is driven out on an LED-A-N pin, the pin floats to a "tri-state" condition and neither of the LEDs light up. This indicates that the respective port is either disabled or nothing is attached

#### Diodes:

**D2000**

* This diode ensures that when any of the LED-A-N pins float to a tri-state condition, the LEDs do not light up, correctly indicating the respective downstream is disabled or nothing is connected

#### Crystals:

**X2000**

* External 24MHz external crystal which provides the clock signal to the USB hub

### Appendix E: Internal Battery Charger Parts Selection and Description

#### Integrated Circuits:

U2100

LTC4007 4A Charger

#### Resistors:

R2100

Low-pass Resistor used to prevent DC overshoot.

* -Value: 10Ω
* -Value based on previous design calculations. Given we are using the same charger chip; keeping the same value seemed reasonable.

R2101

* -Referred to Rsense in LTC4007 datasheet
* -Value 1 mΩ
* -Using equation of I2R = P, 8.52(.001) = .07225

R2102,2103

* -Value: 3.01k
* -Based on LTC4007 datasheet values

R2104,2105,2106,2107,2108,2109,2110

* -Value: 47k
* -Based on need for PIC in previous design
* -value is place holder as PIC need not currently known

R2111,2112

* -The two components added together equal Rprog in LTC4007 datasheet
* -Value: 82.5k
* -Using equation for Rprog, got 82.343k total, previous design had 30.1k and 51.1k, which equals 81.2k , which is close so will add .5k to each to get within range, thus 30.6k and 51.6k respectively.

R2113

* Value: 6.04k
* Based on LTC4007 datasheet

R2114

* Value: 309k
* Using equation found in Rt pin description, gives 2.006 hours timer period, 308k better, but not a standard value.

R2115

* Value: 5k
* Based on value in datasheet, used to calculate Rcl

R2116

* Value : .168 ohms
* Based on 8.5 A current, and equation found in Adaptor limiting section

R2117

* Value: 11.8k
* Located before thermistor

R2118

* Value: 13.5k
* Located in parallel with thermistor

R2119

* Value 10k

#### Capacitors:

C2100

* Bypass capacitor
* Value: 15 nF
* Within range given on ltc4007 charger data sheet

C2101

* Value:.12uF
* Based on value given in ltc4007 charger datasheet

C2102

* Value: .0047uF
* Based on values in LTC charger datasheet

C2103,2104

* Value: 20uF
* Based on values in LTC Charger datasheet diagram

C2105

* Value .1uF
* Based on Value in LTC charger datasheet

C2106

* Value: 1.2uF
* Used equations related to thermistor, found in ltc4007 datasheet, calculated at 1.186 uF
* Digi-key number: [399-3119-2-ND](http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=399-3119-2-ND)

C2107

* Value: 39u
* Battery board

C2108

* Value: .1u

C2109

* Value: 100nF

#### Transistors:

Q2100

* N channel mosfet
* Model #: STS17NH3LL
* Operates RDS 50 mOhms at 8.5A

Q2101,2102

* P channel mosfet
* Model# : FQB17P06
* Operates 120 mOhms at 8.5A

Q2103

* N channel mosfet
* Model#: STS17NH3LL
* Operates RDS 50 mOhms at 8.5A
* Previous model only operated at 4.5A

#### Diodes:

D2100

* Model: MA2Q705
* Based on previous charger circuit design

#### Inductors:

L2100

Value 10uH

Calculated value less than 10uH not recommended in ltc4007 datasheet, but calculated value was.

#### Other:

TVS2100

* Used in previous design

### Appendix F: External Battery Charger Parts Selection and Description

#### Transistors:

Q2114,2115,2116

* See Q2104 for specs
* Used to control flow based on microcontroller signal
* 2115,2116 used for loads

#### Capacitors:

C2117,2118,2119

- See C2107 for details

#### Integrated circuits:

U2111,2112,2113

See U2101 for specifics

Used to control flow based on microcontroller signal

### Appendix G: Battery Sensor Parts Selection and Description

* **D3001-D3005:** LEDs for Fuel-Gauge Display
* **D3006-D3009 and R3006, R3017, R3022 and R3023:** Protection circuits for the input/output data pins.
* **R3007:** Sense resistor for the DS2788. With R3007 = 1mOhm, the current resolution is 1.5626uV/1mOhm = 1.5mA, which is good enough for our test.

The resistor chosen is CSNL10.001FRCT-ND(Digi-Key number).

* Family Chip Resistor - Surface Mount
* Series CSNL
* Resistance In Ohms 0.001
* Power (Watts) 1.5W
* Tolerance ±1%
* Lead Style Surface Mount (SMD - SMT)
* Case 2010 (5025 metric)
* Packaging Cut Tape (CT)
* Composition Current Sense, Metal Foil
* Temperature Coefficient ±50ppm/°C
* **Q1, Q2, R3008-R3011, and C3001**: Q1 is a P-channel FET, and Q2 is a N-channel FET. R3008 and R3009 form a voltage divider circuit to provide the right voltage level for VIN pin. R3010 and R3011 form another voltage divider to provide the right voltage level for Vds of Q1. Before the start of a voltage conversion, VMA is driven high. Then Q2 turns on. As a result, Q1 turns on. Therefore, VIN (the Voltage sense input) will input the voltage, which is one fourth of the total battery pack voltage. At the end of the conversion cycle, the VMA pin is driven low. Then Q1 and Q2 are both off. As a result, VIN doesn't input any voltage data. VMA is the voltage measure active. The capacitor C3001 is used to stabilize voltage change.
* **F3001:** Fuse to protect the circuit when the current is too high. The one chosen is 0456030.ER from Littelfuse Inc. The Digi-Key Part Number is 0456030.ER-ND (3).
* Series NANO²® 456
* Current 30A
* Voltage - Rated 125V
* Package / Case 0.397" L x 0.123" W x 0.123" H (10.1mm x 3.12mm x 3.12mm)
* Fuse Type Fast Acting, Short Time Lag
* Mounting Type Holder/Surface Mount
* Other Names 456030.00
* **R3012-R3015**: Series resistors on each of the cell inputs to reduce the initial current surge through the ISL9208 inputs. From the application node, a series resistance of 15Ohms will add about 1mV of error to the cell voltage reading, which is acceptable.
* **R3016:** Sense resistor of ISL9208 to monitor the change and discharge current. From example 1 of the application note, if the desired over-current level = 8A, and desired short circuit current level = 17A, then the ratio = 17/8 = 2.125. From the table 3, the short circuit threshold is 0.2V and the over-current threshold is 0.10V. The value of the sense resistor = 0.1V/8A = 12.5mOhm.

The resistor chosen is ERJ-B1CJR012U-ND(Digit-Key part number) (3).

* Family Chip Resistor - Surface Mount
* Series ERJ
* Resistance In Ohms 0.012
* Power (Watts) 1W
* Tolerance ±5%
* Lead Style Surface Mount (SMD - SMT)
* Case 2010 (5025 metric)
* Packaging Tape & Reel (TR)
* Composition Thick Film
* Temperature Coefficient ±350ppm/°C
* **R3018 and TR3001**: The fixed resistor and the thermistor form a voltage divider. The TEMPI pin inputs the voltage across the thermistor to determine the temperature of the cells. Then the TEMPI pin drops below TEMP3V/13, an external over-temperature condition exists. Therefore, the resister value needs to be 12 times as the resistance of the thermistor. Since the thermistor we chose has resistance of 10k at 25 Celsius, the value of R3018 is 120Kohm.

The thermistor chosen is NTCS0805E3103JMT by Vishay/BC Components. The Digi-key part number is BC2292CT-ND (3)..

* Family Thermistor - NTC
* Series 2381
* Resistance in Ohms @ 25°C 10K
* B25/85 3570K
* Operating Temperature -40°C ~ 150°C
* Resistance Tolerance 5%
* Value Tolerance 3%
* Power - Max 210m;
* Mounting Type PCB, Surface Mount
* Package / Case 0805 (2012 metric)
* **T1, C3002 and R3019:** T1 is an NPN transistor. The RGO pin connects the emitter of T1 and works in conjunction with the RGC pin to provide a regulated 3.3V. The RGC connects to the base of T1 and provides the control signal for the external transistor to provide the 3.3V regulated voltage on the RGO pin. R3019 is a pull-up resistor, and C3002 is used to stable the voltage changes.
* **R3020 and R3021**: These two resistors control the wake-up threshold of the ISL9208. Their values are calculated using the EQ.1 in the application node. If the wake-up threshold is 3.8V, and the maximum voltage of each cell is 5 and we have a four-cell battery, then R2/(R1+R2) < 0.19. Since R1 determines the current consumption of the circuit, first choose the R1 value as the highest value that is reasonable to use. Let R1 = 1.2Mohm, then R2 = 281.5Kohm. Therefore, R2 = 280Kohm is selected.

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