**Sponsor:** Portland State Aerospace Society

**Academic Advisor:** Richard Tymerski

**PSAS Advisors:** Andrew Greenberg

|  |  |
| --- | --- |
|  |  |

By,

Pierre Djinki,

Varun Arur

Takuya Nomura

*Capstone 2010:*

*PSAS: Flight Computer Carrier Board*

**Table of Content**

1. Introduction……………………………………………………………………………………………3
	1. Features of Flight Computer Carrier Board…………………………………………3
	2. Block Diagram……………………………………………………………………………………4
2. TQM5200 Module……………………………………………………………………………………5
	1. System Components…………………………………………………………………………...5
	2. Ethernet……………………………………………………………………………………………..7
	3. ATA……………………………………………………………………………………………………8
	4. Programmable Serial Controllers (PSC2)……………………………………………10
	5. Universal Serial Bus (USB1)……………………………………………………………….11
	6. USB2 using PSC3……………………………………………………………………………….11
	7. JTAG and Reset………………………………………………………………………………….12
3. Ethernet Connector………………………………………………………………………………...13
	1. Functional Description………………………………………………………………………14
4. Parallel Advanced Technology Attachment (PATA) Drive…………………………17
	1. Functional Description………………………………………………………………………19
5. CAN Transceiver……………………………………………………………………………………..22
	1. Functional Description……………………………………………………………………….22
6. USB Connections and components……………………………………………………………23
	1. Functional Description………………………………………………………………………..26
	2. Integrated Circuits………………………………………………………………………………26
7. Precision Adjustable Current-limited power Distribution Switches…………….27
	1. Functional Description………………………………………………………………………..29
8. Power Supply Connections and components……………………………………………..31
	1. IC Units……………………………………………………………………………………………….32
9. Reference………………………………………………………………………………………………...43

**Introduction**

The Single board computer (TQM5200 from TQ) used on the LV2 Rocket is a PowerPC-based single board computer, specifically chosen because of a "Linux on POWER" grant from IBM that Dr. Massey received a few years back. Its small size (80 X 60mm) and feature load(400 MHz Freescale MPC5200 PowerPC , 64 MB SDRAM / 32 MB FLASH, Lots of peripherals: USB 1.1, CAN, UARTS, PCI, ATA/IDE, SPI, etc) makes it the perfect SBC for the Rocket Avionic. The main downside of this SBC is that it has an array of high density surface mount connectors on the bottom of the board to mount to a “carrier board.”The carrier board used is a giant multi-purpose carrier board that (STK5200) breaks it into a lots of different connectors . The main problem is that the STK5200 is too big and fragile for the LV2. So, the need for a smaller, more robust , compatible with the TQM5200 but yet fully loaded carrier board is the goal of this design project.

The *fc-carrier*is designed to address the needs for a smaller, robust, more compact but yet fully featured flight computer carrier board that will allow easy interfacing with all other Avionics nodes with maximum performance.

**Features of the Flight Computer Carrier Board**

**Power Supply**

Switching power supply (SPS) module takes 20V input from the rocket bus and converts to 3.3V and 5V. The 5V bus is designed to supply the patch antenna through a USB connector and the 3.3V supplies the SBC and other modules on the carrier board. The SPS node is synchronized with a 500kHz clock for noise control. An active protection circuitry with automatic recovery capability from hazardous conditions is designed for the board protection against overvoltage, under-voltage, and over-current events.

**USB interface**

2 full speed, 802.11a compatible Downstream USB 2.0 modules are designed to interface respectively with the Telemetry node through a USB 802.11a adapter and the Inertial Measurement Unit node through the multipurpose Rocketbus Connector.

**CAN interface**

Controller Area Network interfacing is added to meet the need for a highly reliable safety system and communication bus between the nodes of the Avionics system. The peer to peer bus topology nature of CANs in case of power failure for instance will not result in failure of the CAN bus, which is important in critical situations.

**PATA flash drive**

A 44 pin IDE Flash Module provides a reliable storage device that meets the challenges that hostile environment and limited space that the Avionics chamber represent. It is compatible with Standard IDE ATA interface. This module is paired with a 44 pin IDE/ATA embedded Disk card that support UDMA data transfer mode also supported by the LV2 SBC, allowing optimum data transfer speed.

**Ethernet Connector**

A separate off-board Ethernet connector is designed for the sole purpose of optimizing the computer carrier board size. The relatively fast data transfer speed of Ethernet makes it a method of choice for communicating with the Rocket while on the ground.

Ethernet connection provides a direct, low noise area network technology used for fast communication with the flight computer board.

**Block Diagram**

****

Fig. Block Diagram of Flight Computer Carrier Board

**TQM5200 Module**

The TQM5200 has the Freescale PowerPC Processor MPC5200 up to 400MHz with MPC603e Processor Core which includes the following features:

* 33MHz Oscillator for the CPU-Clock
* Silicon Motion Graphic Controller SM501 with 8MB internal graphic memory
* 24MHz Oscillator for the Graphic Controller
* SDRAM: 16MB up to 128MB1 / 256MB2; 32Bit data length
* Flash: 4MB up to 32MB Flash3 Data length : 32Bit
* SRAM: 512kByte or 1Mbyte, data length: 16-Bit. Possibility of buffering the battery by the Basis-Hardware
* Serial EEPROM: 0kBit up to 64kBit, I2C-Bus
* CPLD for Reset-Configuration and activation of SRAM and Graphic-Controller
* Driver for two serial interfaces (RxD, TxD)
* 32-Bit Bus driver and 24-Bit Address Register for module components at the Local-Plus-Bus
* COP/JTAG Interface
* Single Power Supply 3.3V
* Switch-Mode DC/DC Converter on the Module (3.3V on 1.5V)
* Linear DC/DC Converter on the Module (3.3V on1.8V)
* 1.5V Supervisor/Power-Fail-Logic
* 1.8V Supervisor/Power-Fail-Logic
* 3.3V Supervisor/Power-Fail-Logic with SDRAM Battery Backup
* 240 Pin + 80Pin (320Pin) Board-to-Board connector system

This Module is supplied with 3.3V power supply.

**TQM5200 Connector:**

* Two 40 pin connector :
	+ Part Number: [179030-1](http://www.tycoelectronics.com/catalog/pn/en/179030-1)
	+ Connector Style = Plug
	+ 40 Positions
	+ PCB Mount Angle = Vertical
	+ Board-to-Board Stack Height = 7.00 mm, 11.00 mm, 15.00 mm, 19.00 mm
* Two 120 pin connector :
	+ Part Number: [179030-5](http://www.tycoelectronics.com/catalog/pn/en/179030-5)
	+ Connector Style = Plug
	+ 120 Positions
	+ PCB Mount Angle = Vertical
	+ Board-to-Board Stack Height = 7.00 mm, 11.00 mm, 15.00 mm, 19.00 mm

**System Components**

**CPU Main**

* MPC603e series G2\_LE core
* Superscalar architecture
* 760Mips at 400MHz (-40 to +85°C)
* 450Mips at 264MHz (-40 to +105°C)
* 16k Instruction cache, 16k Data cache
* Double precision FPU
* Instruction and Data MMU
* Standard & Critical interrupt capability

**SDRAM / DDR Memory Interface**

* up to 133MHz operation
* SDRAM and DDR SDRAM support
* 256-MByte addressing range per CS, Two CS available
* 32-bit data bus
* Built-in initialization and refresh

**External Bus Interface**

* Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
* 8 programmable Chip Selects
* Non multiplexed data access using 8/16/32 bit data bus with up to 26 bit address
* Short or Long Burst capable
* Multiplexed data access using 8/16/32 bit data bus with up to 25 bit address

**Peripheral Component Interconnect (PCI) Controller**

* Version 2.2 PCI compatibility
* PCI initiator and target operation
* 32-bit PCI Address/Data bus
* 33 and 66 MHz operation
* PCI arbitration function

**ATA Controller**

* Version 4 ATA compatible external interface

**6 Programmable Serial Controllers (PSC)**

* UART or RS232 interface
* CODEC interface for Soft Modem, Master/Slave CODEC Mode, I2S and AC97
* Full duplex SPI mode
* IrDA mode from 2400 bps to 4 Mbps

**Fast Ethernet Controller (FEC)**

* Supports 100Mbps IEEE 802.3 MII, 10Mbps IEEE 802.3 MII, 10Mbps 7-wire interface

**Universal Serial Bus Controller (USB)**

* Version 1.1 Host only
* Support for two independent USB slave ports

**Two Inter-Integrated Circuit Interfaces (I2C)**

* Serial Peripheral Interface (SPI)

**Dual CAN 2.0 A/B Controller (MSCAN)**

* Motorola Scalable Controller Area Network (MSCAN) architecture
* Implementation of version 2.0A/B CAN protocol
* Standard and extended data frames

**Ethernet**

The Ethernet pins are connected to two 10 pin 2mm Single row connectors. The Ethernet daughter board is attached to this connector to use the Ethernet function.

Connector Part Number : *(In Stock with PSAS)*

Note - Pin 7 of J1007 is connected to PO\_RESET

**Ethernet Pin Descriptions and Function**

|  | **Pin**  | **Function**  | **Description**  | **Dir.** |
| --- | --- | --- | --- | --- |
|  | ETH\_0  | ETH\_TX\_EN  | Ethernet Transmit Enable  | I/O  |
|  | ETH\_1  | ETH\_TXD\_0  | Ethernet Transmit Data Output  | I/O  |
|  | ETH\_2  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_3  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_4  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_5  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_6  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_7  | GPIO  | Simple General Purpose Output  | I/O  |
|  | ETH\_8  | ETH\_CD  | Ethernet Carrier Detect  | I/O  |
|  | ETH\_9  | ETH\_RXCLK  | Ethernet Receive Clock  | I/O  |
|  | ETH\_10  | ETH\_COL  | Ethernet Collision Detect Input  | I/O  |
|  | ETH\_11  | ETH\_TXCLK  | Ethernet Transmit Clock Input  | I/O  |
|  | ETH\_12  | ETH\_RXD0  | Ethernet Receive Data Input  | I |
|  | ETH\_13  | INTERRUPT  | INTERRUPT  | I/O  |
|  | ETH\_14  | INTERRUPT  | INTERRUPT  | I/O  |
|  | ETH\_15  | INTERRUPT  | INTERRUPT  | I/O  |
|  | ETH\_16  | INTERRUPT  | INTERRUPT  | I/O  |
|  | ETH\_17  | GPIO  | Simple General Purpose Output with WAKE UP | I/O  |

**ATA**

The Advanced Technology Attachment (ATA) Controller provides full functional compatibility with ATA-4 documentation, supporting Ultra-33. For more ATA Standards information, refer to "American National Standard for Information Technology—AT Attachment with Packet Interface Extension (ATA/ATAPI-4)".

The ATA is connected to Integrated Drive Electronic (IDE) Connector ([DOM EDC4000 IDE 44Pin Horizontal Type A](http://www.memorydepot.com/ssd/listcat.asp?catid=EDC400044A))

**ATA Functions, Local Plus Address/Data Bus signals**

|  | **PIN**  | **ATA Function**  | **Description** |
| --- | --- | --- | --- |
|  | EXT\_AD\_31  | n/a  | n/a  |
|  | EXT\_AD\_30  | n/a  | n/a  |
|  | EXT\_AD\_29  | n/a  | n/a  |
|  | EXT\_AD\_28  | n/a  | n/a  |
|  | EXT\_AD\_27  | n/a  | n/a  |
|  | EXT\_AD\_26  | n/a  | n/a  |
|  | EXT\_AD\_25  | n/a  | n/a  |
|  | EXT\_AD\_24  | n/a  | n/a  |
|  | EXT\_AD\_23  | n/a  | n/a  |
|  | EXT\_AD\_22  | n/a  | n/a  |
|  | EXT\_AD\_21  | n/a  | n/a  |
|  | EXT\_AD\_20  | n/a  | n/a  |
|  | EXT\_AD\_19  | n/a  | n/a  |
|  | EXT\_AD\_18  | ATA\_SA\_2  | ATA Address Bit 2 |
|  | EXT\_AD\_17  | ATA\_SA\_1  | ATA Address Bit 1 |
|  | EXT\_AD\_16  | ATA\_SA\_0  | ATA Address Bit 0 |
|  | EXT\_AD\_15  | ATA\_DATA\_15  | ATA Data Bit 15 |
|  | EXT\_AD\_14  | ATA\_DATA\_14  | ATA Data Bit 14 |
|  | EXT\_AD\_13  | ATA\_DATA\_13  | ATA Data Bit 13 |
|  | EXT\_AD\_12  | ATA\_DATA\_12  | ATA Data Bit 12 |
|  | EXT\_AD\_11  | ATA\_DATA\_11  | ATA Data Bit 11 |
|  | EXT\_AD\_10  | ATA\_DATA\_10  | ATA Data Bit 10 |
|  | EXT\_AD\_9  | ATA\_DATA\_9  | ATA Data Bit 9 |
|  | EXT\_AD\_8  | ATA\_DATA\_8  | ATA Data Bit 8 |
|  | EXT\_AD\_7  | ATA\_DATA\_7  | ATA Data Bit 7 |
|  | EXT\_AD\_6  | ATA\_DATA\_6  | ATA Data Bit 6 |
|  | EXT\_AD\_5  | ATA\_DATA\_5  | ATA Data Bit 5 |
|  | EXT\_AD\_4  | ATA\_DATA\_4  | ATA Data Bit 4 |
|  | EXT\_AD\_3  | ATA\_DATA\_3  | ATA Data Bit 3 |
|  | EXT\_AD\_2  | ATA\_DATA\_2  | ATA Data Bit 2 |
|  | EXT\_AD\_1  | ATA\_DATA\_1  | ATA Data Bit 1 |
|  | EXT\_AD\_0  | ATA\_DATA\_0  | ATA Data Bit 0 |

**ATA Dedicated Signals**

**Signal descriptions**

**LP*CS4 and LP*CS5 - (Chip select, ATA\_CS (1:0))**

These are the chip select signals from the host used to select the Command Block registers (see 7.2). When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

**ATA\_SA (2:0) (Device address)**

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.

**ATA\_DATA (15:0) (Device data)**

This is an 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide.

**ATA\_IOR (Device I/O read: Ultra DMA ready: Ultra DMA data strobe)**

ATA\_IOR- is the strobe signal asserted by the host to read device registers or the data port.

**ATA\_IOW (Device I/O write: Stop Ultra DMA burst)**

ATA\_IOW- is the strobe signal asserted by the host to write device registers or the data port

**ATA\_DACK- (DMA acknowledge)**

This signal shall be used by the host in response to ATA\_DARQ to initiate DMA transfers.

**ATA\_DARQ (DMA request)**

This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK-, i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

**ATA\_INTRQ (Device interrupt)**

This signal is used by the selected device to interrupt the host system. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer and shall be driven either asserted or negated.

When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOR- that reads the Status register. When asserted, this signal shall be negated by the device within 400 ns of the negation of DIOW- that writes the Command register.

When the device is selected by writing to the Device/Head register while an interrupt is pending, INTRQ shall be asserted within 400 ns of the negation of ATA\_IOW- that writes the Device/Head register. When the device is deselected by writing to the Device/Head register while an interrupt is pending, INTRQ shall be negated within 400 ns of the negation of DIOW- that writes the Device/Head register.

**ATA\_IOCHRDY:**

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request. If the device requires to extend the host transfer cycle time at PIO modes 3 and above, the device shall utilize IORDY. Hosts that use PIO modes 3 and above shall support IORDY.

**ATA Pin Description**

|  | **PIN**  | **Function**  | **Reset Value**  | **Description** |
| --- | --- | --- | --- | --- |
|  | **Pin ATA\_DRQ**  |  |  |
|  | ATA  | ATA\_DRQ  | logic 0  | ATA DMA Request |
|  | **Pin ATA\_DACK**  |  |  |
|  | ATA  | ATA\_DACK  | logic 1  | ATA DMA Request |
|  | **Pin ATA\_IOR**  |  |  |
|  | ATA  | ATA\_IOR  | logic 1  | ATA read - 0, no read - 1 |
|  | **Pin ATA\_IOW**  |  |  |
|  | ATA  | ATA\_IOW  | logic 1  | ATA write - 0, no write - 1 |
|  | **Pin ATA\_IOCHDRY**  |  |  |
|  | ATA  | ATA\_IOCHDRY  | logic 1  | ATA negated to extend transfer |
|  | **Pin ATA\_INTRQ**  |  |  |
|  | ATA  | ATA\_INTRQ  | logic 1  | ATA Interrupt Request |
|  | **Pin ATA\_ISOLATION** |  |  |
|  | ATA  | ATA\_ISOLATION  | logic 1  | ATA Levelshifter control signal |

**Programmable Serial Controllers 2 (PSC2)**

The [Controller Area Network (CAN) transceiver](http://psas.pdx.edu/avionics/capstone2010/design/can/) is connected to the PSC2

|  | **Pin Name**  | **Dir.**  | **CAN Function**  | **Description** |
| --- | --- | --- | --- | --- |
|  | PSC2\_0  | I/O  | **CAN1\_TX**  | CAN1\_TX CAN Transmit |
|  | PSC2\_1  | I/O  | **CAN1\_RX**  | CAN1\_RX CAN Receive |
|  | PSC2\_2  | I/O  | **CAN2\_TX**  | CAN2\_TX CAN Transmit |
|  | PSC2\_3  | I/O  | **CAN2\_RX**  | CAN2\_RX CAN Receive Data |
|  | PSC2\_4  | I/O  | **GPIO*w/ WAKE*UP**  | Simple General Purpose I/O with WAKE UP |

**Universal Serial Bus Controller-1 (USB1)**

The USB1 pins are connected to the [USB transceiver](http://psas.pdx.edu/avionics/capstone2010/design/usb/)

|  | **Pin Name**  | **Dir.**  | **USB**  | **Description** |
| --- | --- | --- | --- | --- |
|  | USB\_0  | I/O  | USB1\_OE  | USB Output Enable |
|  | USB\_1  | I/O  | USB1\_TXN  | USB Transmit Negative |
|  | USB\_2  | I/O  | USB1\_TXP  | USB Transmit Positive |
|  | USB\_3  | I  | USB1\_RXD  | USB Receive Data |
|  | USB\_4  | I  | USB1\_RXP  | USB Receive Positive |
|  | USB\_5  | I  | USB1\_RXN  | USB Receive Positive |
|  | USB\_6  | I/O  | USB1\_PORTPWR  | USB Port Power |
|  | USB\_7  | I/O  | USB1\_SPEED  | USB Speed |
|  | USB\_8  | I/O  | USB1\_SUSPEND  | USB Susupend |
|  | USB\_9  | I/O  | USB1\_OVERCNT  | USB Over Current |

**Programmable Serial Controllers 3 (PSC3)**

The second Universal Serial Bus Controller [(USB2) transceiver](http://psas.pdx.edu/avionics/capstone2010/design/usb/) is connected to the PSC3 pins.

|  | **Pin Name**  | **Dir.**  | **USB Function**  | **Description** |
| --- | --- | --- | --- | --- |
|  | PSC3\_0  | I/O  | USB1\_OE  | USB Output Enable |
|  | PSC3\_1  | I/O  | USB1\_TXN  | USB Transmit Negative |
|  | PSC3\_2  | I/O  | USB1\_TXP  | USB Transmit Positive |
|  | PSC3\_3  | I  | USB1\_RXD  | USB Receive Data |
|  | PSC3\_4  | I  | USB1\_RXP  | USB Receive Positive |
|  | PSC3\_5  | I  | USB1\_RXN  | USB Receive Positive |
|  | PSC3\_6  | I/O  | USB1\_PORTPWR  | USB Port Power |
|  | PSC3\_7  | I/O  | USB1\_SPEED  | USB Speed |
|  | PSC3\_8  | I/O  | USB1\_SUSPEND  | USB Susupend |
|  | PSC3\_9  | I/O  | USB1\_OVERCNT  | USB Over Current |

**JTAG (Joint Test Action Group)**

The MPC5200 provides the user an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port. The COP Interface provides access to the MPC5200's imbedded Freescale MPC603e G2\_LE processor. This interface provides a means for executing test routines and for performing software development & debug functions.

The JTAG pins and the Reset pins are connected to a 16 pin 2mm Dual row Connector.

**JTAG Pins**

|  | **PIN**  | **Description** |
| --- | --- | --- |
|  | **JTAG\_TDO**  | JTAG Test Data Out |
|  | **JTAG\_TMS**  | JTAG Test Mode Select |
|  | **JTAG\_TDI**  | JTAG Test Data In |
|  | **JCPU*JTAG*TRST**  | JTAG Reset |
|  | **TEST\_SEL\_0**  | Scan Enable (for production test), PLL*BYPASS -input, CK*STOP - output |
|  | **TEST\_SEL\_1**  | ENID Input in Test Mode (for production test) |
|  | **JTAG\_TCK**  | JTAG Test Clock |
|  | **TEST\_MODE\_0**  | Test Mode Select 0 (for production test) |
|  | **TEST\_MODE\_1**  | Test Mode Select 1 (for production test) |

**Reset Pins**

|  | **PIN**  | **Description** |
| --- | --- | --- |
|  | !HRESET  | Hard Reset |
|  | !SRESET  | Soft Reset |
|  | !PO\_RESET  | Power On Reset |
|  | !RESIN  | Reset |

**JTAG/Reset Connector Pin Configuration**

Connector Part Number : [87758-1616](http://search.digikey.com/scripts/DkSearch/dksus.dll?lang=en&site=US&WT.z_homepage_link=hp_go_button&KeyWords=WM18839-ND&x=0&y=0)

|  | **Pin**  | **Function** |
| --- | --- | --- |
|  | 1  | 3.3V |
|  | 2  | JTAG\_TDO |
|  | 3  | JTAG\_TMS |
|  | 4  | JTAG\_TDI |
|  | 5  | JCPU*JTAG*TRST |
|  | 6  | TEST\_SEL\_0 |
|  | 7  | TEST\_SEL\_1 |
|  | 8  | JTAG\_TCK |
|  | 9  | TEST\_MODE\_0 |
|  | 10  | TEST\_MODE\_1 |
|  | 11  | !HRESET |
|  | 12  | !SRESET |
|  | 13  | !PO\_RESET |
|  | 14  | !RESIN |
|  | 15  | GND |
|  | 16  | GND |

**Reference**

* [TQM5200 Hardware Manual](http://psas.pdx.edu/avionics/capstone2010/design/TQM5200.HWM.204.pdf)
* [MPC5200 User Manual](http://psas.pdx.edu/avionics/capstone2010/design/MPC5200UM.pdf)

**ETHERNET CONNECTOR**

**Overview**

The purpose and reason behind the design of a separate Ethernet connector to interface with the flight computer carrier board was the economy of space. Because the flight computer carrier board was to be minimized in size, while still keeping lots of essential features hence components, we decided to design the ethernet as an off board module since it didn't really to be on the board while in flight.

**Part Description**

**Ethernet Transceiver**

Part #: [DP83848C](http://www.national.com/pf/DP/DP83848C.html#Overview)

DIGIKEY Part#: [DP83848CVV-ND](http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=DP83848CVV-ND)

Unit Price: $6.8

Package: 48-LQFP

DC Input Voltage: 3V~3.6V

**RJ45**

Part #: [J1026F21CNL](http://ww2.pulseeng.com/products/datasheets/J402.pdf)

DIGIKEY Part#: [553-1351-ND](http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=553-1351-ND)

Unit Price: $6.59

Package: Panel Mount; Through Hole, Right Angle

Speed: 10/100 Base-TX

LED Color: Yellow - Green

**Crystal Oscillator**

Part #: [ECS-250-20-33-TR](http://www.ecsxtal.com/store/pdf/ecx-32.pdf)

DIGIKEY Part#: [XC1142DKR-ND](http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=XC1142DKR-ND)

Unit Price: $3.57

Frequency: 25Mhz

Mounting Type: Surface mount

***LED***

Part #: LG L29K-G2J1-24-Z

DIGIKEY Part#: [475-2709-2-ND](http://search.digikey.com/scripts/DkSearch/dksus.dll?Detail&name=475-2709-2-ND)

Color: Green

Unit Price: $.16

Forward Voltage: 1.7V

Current: 2mA

**Functional Description**

**Integrated Circuits**

***IC1***

Chosen for its relatively small size (7mmx7mm). Low power consumption, availability of feature such as Media Independent Interface (MII) as well as Auto-MDIX for automatic detection of required cable; it also supports 10Mb/s and 100Mb/s data transfer mode as well as Half/Full-Duplex data transfer mode which are all supported by the MPCxxx.

***XTAL***

This external surface mount crystal oscillator is a 25Mhz crystal (recommended by the Ethernet Transceiver datasheet)

***LED1***

The LED is SPEED LED. It indicates the speed of the device. It would turn on to indicate 100Mb/s and stay off to indicate 10Mb/s

**Resistors**

***R1, R2, R11***

These resistors are used to strap the device to operate in AUTO NEGOTIATION WITH 10/100 HALF/FULL DUPLEX ADVERTISED mode. This mode allows the device to select the most efficient data transfer speed and type, as opposed to the FORCED mode. The datasheet recommend to use 2.2k for strapping resistor values.

***R3***

This is a current limiting resistor. **R3=(3.3V-1.7V)/2mA**, (LED Forward voltage=1.7V, Forward current = 2mA)

***R4***

This resistor is a 4.87k pull down resistor. It's a bias resistor connected to pin 24 (RBIAS) of the Ethernet transceiver. It's value is recommended by the transceiver datasheet.

***R5, R6, R7, R8***

These resistors are impedance matching resistors for a twisted pair interface. Their values were strictly picked out of the datasheet.



***R9 and R10***

These 2.2k are pull up resistor to the 3V3 source connected to pin 20, 21 as recommended by datasheet

***R12***

This is a zero ohm resistor (optional).

**Capacitors**

***C1, C10, C11***

Used as decoupling capacitors for noise suppression at the power pins of the transceiver.

***C2, C3, C4, and C5***

These capacitor values were chosen to be same as the model used on the datasheet.

***C6, C7, C8, C9***

These capacitors are noise suppression capacitor connected to Power Feedback Output and Input pins. Their values were picked strictly with respect to the datasheet recommendation. It is recommended to use a tantalum capacitor for C6; and to connect C6 and C7 as close as possible to the Power Feedback Output pin 23.

***C13, C14***

Load capacitor of the crystal with 20pF capacitance.

***Schematic***



**Parallel Advanced Technology Attachment (PATA) Flash Drive**

**Overview**

Disk on Module (DOM) are flash drives with either 40 or 44 pins IDE/Standard ATA Interface USB or SATA Interface to be used as a computer hard disk drive (HDD). The flash-to-IDE converter simulates a harddisk, and therefore the modules can be used without additional software or drivers. DOMs are highly reliable as they do not have any moving parts like regular hard disks and are small in size and light in weight. However, after a disk crash in traditional hard disk, some data may still be recoverable by scanning the physical media using specialized equipment, but there is no known method to recover lost data from a physically damaged DOM. Currently storage capacities range from 32MB to 32GB with various form factor including vertical or horizontal orientation. The DOM is generally plugged directly to the motherboard.[1]

**Part Description**

Part #: [DOM EDC4000 IDE 44Pin Horizontal Type A](http://www.memorydepot.com/ssd/listcat.asp?catid=EDC400044A) is comprised of a 44 pin embedded disk card and a IDE interface platform

Unit Price: $91.000

Interface: 44pin IDE/ATA

IDE Transfer Mode: PIO mode 0-4/UDMA mode 0-4

Burst Speed Rate: 66.6MB/sec.

Operation Temp: -10Â°C~+70Â°C(Standard)

Vibration: 5G(7~2000Hz)

Shock: 50G/10ms

MTBF: >3,000,000 hours

Read/Write : 80/75Mbs

R/W Endurance: 2,000,000 times

DC Input Voltage: 3.3V-5V

**ATA-TQM pinouts**

| **40 Pin #**  | **ATA-4 PIN NAME**  | **ATA-4 HOST CONNECTION**  | **Host <> Device**  | **STK sheet 5 name**  | **TQM name**  | **PCB requirements**  |
| --- | --- | --- | --- | --- | --- | --- |
| 1  | RESET-  | “  |  | IDE\_RESET-  | ATA\_RESET  |  |
| 2  | Ground  | GND  |  | GND  |  |  |
| 3  | DD7  | “  | <> \*  | IDE5V\_DD7 (10K pulldown)  | EXT\_AD7  | 10K pulldown  |
| 4  | DD8  | “  | <> \*  | IDE5V\_DD8  | EXT\_AD8  |  |
| 5  | DD6  | “  | <> \*  | IDE5V\_DD6  | EXT\_AD6  |  |
| 6  | DD9  | “  | <> \*  | IDE5V\_DD9  | EXT\_AD9  |  |
| 7  | DD5  | “  | <> \*  | IDE5V\_DD5  | EXT\_AD5  |  |
| 8  | DD10  | “  | <> \*  | IDE5V\_DD10  | EXT\_AD10  |  |
| 9  | DD4  | “  | <> \*  | IDE5V\_DD4  | EXT\_AD4  |  |
| 10  | DD11  | “  | <> \*  | IDE5V\_DD11  | EXT\_AD11  |  |
| 11  | DD3  | “  | <> \*  | IDE5V\_DD3  | EXT\_AD3  |  |
| 12  | DD12  | “  | <> \*  | IDE5V\_DD12  | EXT\_AD12  |  |
| 13  | DD2  | “  | <> \*  | IDE5V\_DD2  | EXT\_AD2  |  |
| 14  | DD13  | “  | <> \*  | IDE5V\_DD13  | EXT\_AD13  |  |
| 15  | DD1  | “  | <> \*  | IDE5V\_DD1  | EXT\_AD1  |  |
| 16  | DD14  | “  | <> \*  | IDE5V\_DD14  | EXT\_AD14  |  |
| 17  | DD0  | “  | <> \*  | IDE5V\_DD0  | EXT\_AD0  |  |
| 18  | DD15  | “  | <> \*  | IDE5V\_DD15  | EXT\_AD15  |  |
| 19  | Ground  | GND  |  | GND  |  |
| 20  | (keypin) | NC  |  | NC (key pin)  |  |
| 21  | DMARQ  | “  | <  | IDE5V\_DMAREQ  | ATA\_DRQ  | 10K pulldown  |
| 22  | Ground  | GND  |  | GND  |  |
| 23  | DIOW-:STOP  | “  |  | IDE*5V*IOW  | !ATA\_IOW  |  |
| 24  | Ground  | GND  |  | GND  |  |
| 25  | HDMARDY-  | “  |  | IDE5V\_IOR  |  | !ATA\_IOR  |
| 26  | Ground  | GND  |  | GND  |  |  |
| 27  | DDMARDY-  | “  | <  | IDE5V\_IOCHDRY  | ATA\_IOCHDRY  | 1K pullup to 5V  |  |
| 28  | CSEL  | GND  |  | Slave/Master (330 pulldown)  |  | 330 pulldown  |  |
| 29  | DMACK-  | “  |  | IDE*5V*DACK  | !ATA\_DACK |  |  |
| 30  | Ground  | GND  |  | GND  |  |  |  |
| 31  | INTRQ  | “  | <  | IDE5V\_INTHD  | ATA\_INTRQ +  |  |  |
| 32  | reserved  | NC  |  | NC (NP 0R0 to !IDE5VIO16)  |  |  |
| 33  | DA1  | “  |  | IDE5V\_DA1  | EXT\_AD17  |  |  |
| 34  | PDIAG-  | NC  |  | !IDECBLIDFP  | NC  | 100k pulldown & 47n cap  |
| 35  | DA0  | “  |  | IDE5V\_DA0  | EXT\_AD16  |  |  |
| 36  | DA2  | “  |  | IDE5V\_DA2  | EXT\_AD18  |  |  |
| 37  | CS0-  | “  |  | IDE5V\_CS0  | !LP\_CS4  |  |  |
| 38  | CS1-  | “  |  | IDE5V\_CS1  | !LP\_CS5  |  |  |
| 39  | DASP-  | NC  |  | IDE\_HDACT (also to FLACT)  | NC  |  |
| 40  | Ground  | GND  |  | GND  |  |  |
| 41  | VCC - Logic | VCC  |  | VCC\_5VP  |  | 100u + 100n bypass  |  |
| 42  | VCC - Motor | VCC  |  | VCC\_5VP  |  | 100u + 100n bypass  |  |
| 43  | GND  | GND  |  | GND  |  |  |
| 44  | NC  | NC  |  | NC  |  |  |

**Functional Description**

**Transistors**

*Q4*

Manufacturer part#: BSS84

Digi-key part#: BSS84P L6327

Package: SOT-23

Voltage threshold @ Id: 2V @ 20µA

Unit Price: $0.4600

This part was chosen for its low threshold voltage and its availability on digikey

**Transistors**

*Diode*

LED11011 is a Green Led (per Andrew).

*Q1006*

The NTR4101P is a P-Channel Mosfet (Per Andrew)

**Resistors**

*R1046*

This is a current limiting resistor with calculated value 470 Ohm.

*R1105*

*R1040*

CSEL pin is connected to ground through this resistor. Its value was chosen to match the value found on the STK5200 schematic

*R1041*

Used for impedance matching between driver and device, this pull up resistor value was increased from 1kohm to 4.7Kohm (per Andrew)for noise margin improvement i suppose.

*R1042*

A 10K pulled down resistor is required at the host (DMARQ pin.) (**Not sure why we have a 4.7K instead**)

*R1106*

A 10K pulled down resistor is required at the host (INTRQ pin.)

*R1045*

The ATA Spec recommends using either a PU or PD 10kohm resistors at pin DD7 for UDMA configuration as shown below in the schematic from the ATA-SPEC (Rev 18) attached below

*R1047,R1049,R1057,R1058-R1068, R1050-R1056, R1094-R1100,*

These resistors are used for impedance matching. In fact, according to the ATA-4 Spec, careful impedance matching between the host and the connected device is required for proper UDMA operation. Their values were directly taken from Table 5 of the ATA-4 Spec and listed down below.

| **Signal**  | **Host Termination**  | **Device Termination**  |
| --- | --- | --- |
| HDMARDY  | 22 ohm  | 82 ohm  |
| STOP  | 22 ohm  | 82 ohm  |
| CS0-, CS1-  | 33 ohm  | 82 ohm  |
| DA0, DA1, DA2  | 33 ohm  | 82 ohm  |
| DMACK-  | 22 ohm  | 82 ohm  |
| DD[10:0]  | 33 ohm  | 33 ohm  |
| DMARQ  | 82 ohm  | 22 ohm  |
| INTRQ  | 82 ohm  | 22 ohm  |
| DDMARDY-  | 82 ohm  | 22 ohm  |
| RESET-  | 33 ohm  | 82 ohm  |

**Capacitors**

*C1038, C1039*

These are bypass capacitors used for noise attenuation at VCC. Using two capacitors of different values allows selective attenuation of noise at different frequencies (low frequency noise and high frequency noise...)

Their values were picked to reflect the original design on the STK5200.

**Resources and References**

[ATA SPEC](http://psas.pdx.edu/avionics/capstone2010/design/www.t10.org/t13/project/d1153r18-ATA-ATAPI-4.pdf)

[BSS84](http://www.infineon.com/dgdl/BSS84P_Rev2.4.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a304412b407950112b42aa30b43c0)

[1] Wikipedia

**CAN TRANSCEIVER**

* Manufacturer part#: SN65HVD235
* Digi-key part#:SN65HVD235DG4-ND
* Package: SOIC
* Voltage Input: 3-3.6V
* Unit Price:$4.3400

**Functional Description**

**Pins**

Connecting the RS pin (pin 8) to ground through resistor R1022 allows us to select high speed as our mode of operation.

**Integrated Circuits**

***U1008***

This is the Controller Area Network transceiver.

**Resistors**

***R1022***

This resistor sets the slope of the rise and fall of the driver output signal.

For this project we simply used the design the 2009 Capstone team used (we didn't see a need for changing it.)

In that design, they chose the value of R1022 to be **18K** which can be deduced from the graph of the Driver Output Signal Slope vs Slope Control Resistance Value (fig 31 on datasheet)



***R1025***

Bus termination is used to minimize signal reflection on the bus and improve EMC performance. ISO-11898 requires that the CAN bus have a nominal characteristic line impedance of 120Ω. Therefore, the typical terminating resistor value for each end of the bus is 120Ω.[1] (Not sure why a 60 Ohm resistor was recommended instead.)

**Capacitors**

***C1030***

This is a bypass capacitor for noise suppression, burst smoothing between Vcc and GND

***Note***

The whole block made up of *U1007*, *C1028*, *C1029*, *R1024*, *R1023*, *R1021*, *D1000D* and *D1001D* were entirely adopted from the 2009 Capstone.

***Reference:***

[1] ww1.microchip.com/downloads/en/AppNotes/00228a.pdf

**USB Connections and components**

**Overview**

There are 2 downstream USB modules designed to receive and transmit serial data at full speed. One module is made up of a USB transceiver(mfg part# TUSB1106) and a Power-Distribution switch (mfg part# TPS 2552). The second USB block only had the transceiver (mfg part# TUSB1106.)

*The TUSB1106 was chosen over other USB transceivers because of it's availability on DigiKey, it's unambiguous implementation for* *this specific project (it didn't require additional setting for differential mode data transfer) and it's well detailed* *datasheet.*

*The choice for the TPS2552 was a recommendation from Andrew. Moreover, i found the datasheet very detailed and fairly easy* \* to understand. \*

**Universal Universal Serial Bus Transceiver**

* Manufacturer part#: TUSB1106PWR
* Digi-key part#: 296-21923-2-ND
* Package: 16-TSSOP
* Protocol: USB2.0
* Voltage Supply: 1.65V-3.6V
* Unit Price: $8.93

**Pin Description**

The Pin description below were extracted from the datasheet.

**VCCIO**

Supply voltage for digital input/ouput pins (1.65 to 3.6V). This pin must never exceed Vreg voltage

**VREG**

Internal regulator option. Regulated supply-voltage output (3 V to 3.6 V) during 5-V operation. A decoupling capacitor of at least 0.1 mF is required for the regulator bypass option. Used as a supply-voltage input for 3.3 V ± 10% operation.

**VCC**

Supply-voltage input (4 V to 5.5 V). Connect to Vreg(3.3). Can be connected directly to USB supply VBUS regulator bypass option.

**VPU**

Pullup supply voltage (3.3 V ± 10%). Connect an external 1.5-kΩ resistor on D+ (full speed) or D– (low speed). Pin function is controlled by input SOFTCON. SOFTCON = LOW – Vpu(3.3) floating (high impedance), ensures zero pullupcurrent SOFTCON = HIGH – Vpu(3.3) = 3.3 V, internally connected to Vreg(3.3)

**D+**

Positive USB data bus connection

**D-**

Negative USB data bus connection

**/OE**

Output enable (CMOS level with respect to VCC(I/O), active LOW). Enables the transceiver to transmit data on the USB bus input pad.

**SPEED**

Speed selection pin. Adjusts slew rate of differential outputs D+ and D- according to the transmission speed. For full speed (12Mbits/sec)

**SOFTCON**

Software controlled USB connection. Software-controlled USB connection. A HIGH level applies 3.3 V to Vpu(3.3), which is connected to an external 1.5-kΩ pullup resistor. This allows USB connect/disconnect signaling to be controlled by software input pad. Push pull, CMOS

**RCV**

Differential data receiver (CMOS level with respect to VCC(I/O)). Driven LOW when input SUSPND is HIGH. The output state of RCV is preserved and stable during an SE0 (SINGLE ENDED 0) condition output pad.

**VMO**

Driver data (CMOS level with respect to VCC(I/O), Schmitt trigger). Refer to Driving Function Table (pin OE = L) on datasheet using differential input data interface for TUSB1105 (pin MODE = H) and TUSB1106 input pad. Push pull, CMOS.

**VPO**

Driver data (CMOS level with respect to VCC(I/O), Schmitt trigger). Refer to Driving Function Table (pin OE = L) on datasheet using differential input data interface for TUSB1105 (pin MODE = H) and TUSB1106 input pad. Push pull, CMOS.

**VP**

Single-ended D+ receiver (CMOS level with respect to V). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to VCC(5.0) and Vreg(3.3) output pad.

**VM**

Single-ended D- receiver (CMOS level with respect to V). For external detection of single-ended zero (SE0), error conditions, speed of connected device. Driven HIGH when no supply voltage is connected to VCC(5.0) and Vreg(3.3) output pad.

**GND**

Ground Supply

**SUSPND**

A HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a low-level input pad. Push pull, CMOS.

**Functional Description**

**Pins**

In order to bypass the internal regulator inside U1005 and U1006 (TUSB1106), Vreg and Vcc are both connected to the 3.3V power supply and decoupled with a 100nF capacitor to ground. This turns off the voltage regulator, thus enabling power saving.

Vccio should be independently connected to the 3.3V source (TUSB1106 datasheet recommendation pp6)

Pin SOFTCON should be set high to pull Vpu to the 3.3V at the output of the internal regulator through resistor R1014 connected to D+ for full speed configuration.

This pin is connected to PSC1\_0 which is a simple GPIO pin on the MPC5200, and should be enabled for usage in the GPS simple GPIO Enable Register (Ref Section 7.3.2.1.2 on MPC5200B Users Guide, Rev. 1)

**Integrated Circuits**

***U1006***

U1006 from Texas Instrument is a Universal Serial Bus Specification REV.2.0 compliant transceiver designed to allow an easy handling of universal serial bus data transfer by the MPC5200. It is designed to work in full speed mode (12 Mbit/s) with flexible I/O voltage range from 1.65V to 3.6V which allows us to use the 3.3V power internally supplied on the STKxxx. The TUSB1106 allows only differential input mode which is the data transfer mode of choice required for this project; so no additional configuration were needed as with other transceivers (TUSB1105). U1006 is connected to the multipurpose Rocketbus connector which is the main connector of the Generic Front End node designed by the [2009 Capstone](http://psas.pdx.edu/capstone2009/design/node/) that provides interfacing between Flight Computer and the IMU module(Inertial Measurement Unit), the Avionics Power System module, GPS module, and Recovery module.

***U1005***

U1005 which is the other TUSB1106 is used with a power distribution switch (*TPS2552*) provides a second full speed USB compatible with USB Specification Rev.2.0 to connect the Flight Computer to the 802.11a USB adapter on the Telemetry Module

**Resistors**

***R1107-R1110***

These resistors are used for downstream configuration of the USB and for proper operation of D-/D+ data-bus in differential transfer mode. Their values were chosen as recommended by the datasheet.

The TUSB1106 datasheet recommends **15kOhm** for these resistors

**R1016, R1017, R1019 and R1020**

These resistors are driver impedance matching resistors. The cable impedance must match the impedance of the high-speed and full-speed drivers. USB uses differential output driver to drive USB data signal onto the USB,so the driver impedance is very important in assuring optimal transfer of data. The USB Spec Rev2.0 says that When the full-speed driver is not part of a high-speed capable transceiver, the impedance of each of the drivers (ZDRV) must be between 28 Ω and 44 Ω, i.e., within the gray area in Figure 7-4 (on the USB Spec Rev2.0.)

The TUSB1106 datasheet recommends to use **33 Ohms** resistors which complies with the USB Spec Rev2.0

**Capacitors**

***C1019 and C1035***

Used as decoupling capacitors for electrical noise suppression between the power supply and pins Vreg and Vcc on both U1005 and U1006.

***C1019, C1019, C1035, and C1036***

These are used as decoupling capacitors for electrical noise suppression between the power supply and Vccio, Vreg and Vcc on both U1005 and U1006.

The value chosen for both is **100nF (.1uF)** (recommended by TUSB1106 datasheet) which will handle the high frequencies noise signals.

**Precision Adjustable Current-Limited Power-Distribution Switches**

* Manufacturer part#:TPS2552
* Digi-key part#:TPS2552DBVR-ND
* Package: SOT-23-6
* Voltage Input:2.5 ~ 6.5 V
* Unit Price: $9.9800

**Pin Description**

**IN**

Input voltage; connect a 0.1 uF or greater ceramic capacitor from IN to GND as close to the IC as possible.

**OUT**

Power-switch output

**ILIM**

External resistor used to set current-limit threshold;

**/FAULT**

Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions

**EN**

Enable input, logic high turns on power switch

**GRD**

Ground connection; connect externally to PowerPad

**PowerPAD™**

Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

**Functional Description**

**Pins**

**Integrated Circuits**

***U1004***

The U1004 (TPS2552) is a precision adjustable current-limited power-distribution switch from TI with operating range between 2.5V and 6.5V(allowing the use of 3.3V on board power supply) that provides the second downstream USB connecting the flight computer to the Telemetry node with a well regulated power source and a programmable current limit threshold between 75mA and 1.3A via an external resistor whose value will determine the threshold level designed for current protection. It is also built for over-temperature and reverse voltage protection.

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typ) for 4-ms (typ).

Choice of U1004 was recommended by Andrew (i believe one of the reasons was there was already an existing library part for it.)

**Resistors**

***R1111***

This resistor is used to ensure logic level unambiguity at input of EN pin when no signal is received.

***R1012***

This is the open-drain external pull up resistor from 5V VCC to FAULT pin on the TPS2552. Its value is 10Kohm (strong recommendation of TPS2552 datasheet) which gives us a continuous FAULT sink current of .2mA (which is well within the recommended operating condition of 0<=I<=10mA)

***R1013***

This resistor function is to set the Overcurrent Threshold. The recommended 1% resistor should be within the range of 19.1 kΩ ≤ RILIM ≤ 232 kΩ.

The choice of R1013 depends on the design goal such as a design above or below the current limit threshold. **I chose a design above the minimum current limit, because it will ensure start up into full load or heavy capacitive loads.**

The datasheet recommends two methods of selecting R1013. The first is to use the Current-Limit Threshold vs Rilim curve shown below (from datasheet) to find the intersection of RILIM and the maximum desired load current on the IOS(min) curve and choose a value of RILIM below this value.



The second method is to use equations below:

**Ios(min)(mA)=[25230V/[Rilim]^1.016 (kohm)]**

Then we select the closest 1% resistor below the calculated value.

With **Ios(min)=500mA, we get Rilim=46.4 kohms** which will give us a current limit of: **Ios=22980/(Rilim^0.94)=616mA**

This value of current is too high for our design, so i used trial and error in conjunction with table 1 shown below (from datasheet). Common Rilim Resistor Selection on the datasheet to come up with a value of Rilim that will get us as close to 500mA as possible (which is by the way the max current the usb should source.)

**Rilim=57.5 kohms which yields a 509.6 mA current limit.**



**Capacitors**

***C1017***

This is the input decoupling capacitor from IN to GND used for local noise decoupling. It reduces ringing on the input due to power supply transients.

This capacitor is **100uF** ceramic capacitor which is above the recommended range (>= 0.1uF)

***C1018***

This capacitor value is a USB requirement. It's an electrolytic capacitor used for electrical noise attenuation between the + 5V Vbus line and OUT pin of U1004.

Value is **100nF.**

**Power Supply Connections and Components**

**Figuring out front end current consumption**

What's the power consumption of the flight computer carrier board? Roughly, it's the components of the TQM5200, the Innodisk flash HDD, running the secondary USB which can take up to 500 mA, and the various other misc circuits (debugging LEDs, clock dividers, USB transceivers, CAN transcevers, etc).

| **Component**  | **V**  | **I**  | **P**  | **I @ Vbat = 10V @ 70%** |
| --- | --- | --- | --- | --- |
| TQM5200  | 3.3 V  | 1.96 A  | 6.47 W  | 0.924 A |
| INNOdisk  | 3.3 V  | 0.14 A  | 0.46 W  | 0.066 A |
| USB-2  | 5.0 V  | 0.50 A  | 0.25 W  | 0.179 A |
| Misc  | 3.3 V  | 0.25 A  | 0.83 W  | 0.118 A |
| **TOTAL**  |  |  |  | **1.29 A** |

So the power supply front end should be able to handle 1.3 A continuously.

**IC Units**

* **UXXXX: LTM4619 (Dual, 26VIN, 4A DC/DC μModule Regulator)**
	+ Description: This is SPS which creates 5V and 3.3V output from 10-20V input. This component was chosen because of high current output (4A) and simplicity of design. It has inductors in the module thus we do not need to design whole buck converter. SPS is synchronized with external clock of 500kHz from the 24MHz oscillator on TQM5200. 24MHz signal is divided down to 500kHz through U1009 and U1010. See those components notes. Its’ input current and output voltage is protected by Q1000. 500kHz of external was chosen because it is easier to be generated from 24MHz oscillator using frequency divider.
	+ **UXXXX: LTM4619 Pin Description**

| **Pin Name**  | **Description** |  |
| --- | --- | --- |
| Vin  | Protected power is supplied decoupled with 2 10uF capacitors. |  |
| Vout1  | Output 5V, 500mA decoupled with 100uF |  |
| Vout2  | Output 3.3V, 2.2A decoupled with 100uF |  |
| PGND  | Power ground: Just connect to ground. |  |
| INTVcc  | Internal 5V regurator we don't use this. |  |
| EXTVcc  | This is only required when Vin<6V, so we float this pin. |  |
| SGND  | Signal ground, just connected to ground. |  |
| MODE/PLLIN  | We use this pin as PLLIN of 500kHz. (clock is supplied from clystal oscillator on TQM5200) |  |
| FREQ/PLLFLTR  | Since we use external clock, we leave this pin unconnected. |  |
| TK/SS1  | 0.2nF capacitor is connected to set soft-start time 123us. (tsoft-start=0.8V\*Css/1.3uA) |  |
|  |  |  |
| TK/SS2  | 0.2nF capacitor is connected to set soft-start time 123us.(tsoft-start=0.8V\*Css/1.3uA) |  |
| VFB1  | R1000 (11.5kΩ) is used to program 5V output voltage on Vout1. Refer table1 of datasheet |  |
|  |  |  |
| VFB2  | R1001 (19.1kΩ) is used to program 3.3V output voltage on Vout2. Refer table1 of datasheet |  |
|  |  |  |
| COMP1  | Current Control Threshold Noconnection Followed typical application. |  |
| COMP2  | Current Control Threshold Noconnection Followed typical application.  |  |
| PGOOD  | Only connected to test point because we do not care. |  |
| RUN1  | Floated to enable Vout1 |  |
| RUN2  | Floated to enable Vout2 |  |
| SW1  | Test pin to check operation frequency |  |
| SW2  | Test pin to check operation frequency |  |
|  |  |  |

* **U1001: MAX5902AAETT (+72V SOT23 Simple Swapper Hot-Swap Controller)**
	+ Description:This hot-swap controller IC serves two purposes: (1) circuit-breaker and (2) UVLO protection. This controller turns off Q1000 under several conditions. (1) if there is under voltage at the input, (2) if there is overcurrent, (3) if the die temperature exceeds +125 C (4) if SPS-5V output exceeds 5.46V and (5) if SPS-3.3V output exceeds 3.6V.

	\*Note
	(1) Under voltage protection threshold is set to be 9V by voltage divider R1103 and R1104.
	(2) Over current threshold of 1.62A is set by series resistance of R1002 and RDS(on) of Q1000.
	(4) Overvoltage protection of SPS-5V is sensed by U1003 and toggled by Q1001.
	(5) Overvoltage protection of SPS-3.3V is sensed by U1002 and toggled by Q1002.
	+ Justification:We use the same part from capstone 2009[LV2C:GFE:U2250]
	However we reduced some functionalities.(1)PGOOD is not used in our circuit because we do not care PGOOD signal durling launch.(2)We do not have MOSFET connected to ON/OFF pin because we do not let microcontroller to toggle circuit breaker.
	+ **U1001: MAX5902AAETT Pin Description**

| **Pin Name**  | **Description** |
| --- | --- |
| ON/OFF  | Connected to UVLO resistor divider network R1103 and R1104. Their value were selected to set UVLO voltage to be 9V. See R1103  |  |
| VS  | Monitors voltage dropp across Q1000 |  |
| DRAIN  | Monitors voltage dropp across Q1000 |  |
| GATE  | Used to shut off Q1000 |  |
| PGOOD  | We do not use PGOOD |  |
| GND  | Connected to ground |  |

* **U1002: TLV3012AIDBVT (Comparator with Voltage Reference)**
	+ Description: U1002 watches overvoltage on SPS-3.3V output. In the event SPS-3.3V output exceeds 3.6V, it turns on Q1002 and makes pin2 (Drain) of U1001 close to GND, then U1001 shuts Q1000 off: SPS is disconnected from power bus. See capstone 2009 [LV2C:GFE:U2251].
	+ Justification: We use the same part from capstone 2009[LV2C:GFE:U2250]
	+ **U1002: TLV3012AIDBVT Pin Description**

| **Pin Name**  | **Description** |
| --- | --- |
| V+  | Connected to C1010 which act like a power supply to avoid power cycling when SPS output decline to certain level. 2.7uF capacitor was chosen to store charge more than 0.5s. See C1010. |  |
|  |  |  |
| REF  | integrated voltage reference |  |
| IN-  | Use REF(1.242V) for voltage reference |  |
| IN+  | Connected to the voltage divider which programs overvoltage shut down threshold at 3.6V for SPS-3.3V. See R1005 and R1007. |  |
| V-  | Ground |  |
| OUT  | Used to switch Q1002 which shut off the breaker when overvoltage occurs |  |

* **U1003: TLV3012AIDBVT (Comparator with Voltage Reference)**
	+ Description: U1003 watches overvoltage on SPS-5V output. In the event SPS-5V output exceeds 5.46V, it turns on Q1001 and makes pin2 (Drain) of U1001 close to GND, then U1001 shuts Q1000 off: SPS is disconnected from power bus. See capstone 2009 [LV2C:GFE:U2251].
	+ Justification: We use the same part from capstone 2009[LV2C:GFE:U2250]
	+ **U1003: TLV3012AIDBVT Pin Description**

| **Pin Name**  | **Description** |
| --- | --- |
| V+  | Connected to C1012 which act like a secondary power supply to avoid power cycling when SPS output drops down by certain level. 2.7uF capacitor was chosen to store charge more than 0.5s. See C1012. |  |
|  |  |  |
| REF  | integrated voltage reference |  |
| IN-  | Use REF(1.242V) for voltage reference |  |
| IN+  | Connected to the voltage divider which programs overvoltage shut down threshold at 5.46V for SPS-5V. See R1006 and R1008. |  |
| V-  | Ground |  |
| OUT  | Used to switch Q1001 which shut off the breaker when overvoltage occurs |  |

* **U1009: SN74LVC2G80DCU (Dual positive-edge-triggered D-type Flop-flop)**
	+ Description: This D-type flip-flops divide 24MHz clock signal from TQM5200 by 4, and it is cascaded to U1010 (SN74LS92D: divide by 12 counter) to finally create 500kHz clock. Since we did not know output voltage levels of 24MHz oscillator on TQM5200, and to ensure this clock drives flip-flops, we had to use the same supply voltage (3.3V) for this component. Output voltage level (Running at 3.3V supply) of this component also had to meet input voltage levels of U1010 (SN74LS92D: divide by 12 counter).
	+ **U1009: SN74LVC2G80DCU Pin Description**

| **Pin Name**  | **Description** |
| --- | --- |
| 1CLK  | Connected to 24MHz oscillator (input of the first divide by 2 flip-flop) |  |
| 1D  | '#1Q is fedback to this pin to function as a divide by 2 flip-flop |  |
| '#1Q  | Feedback for 1D, this pin is also connected to input of the second divide by 2 flip-flop) |  |
| 2CLK  | input of the second divide by 2 flip-flop |  |
| 2D  | '#2Q is fedback to this pin to function as a divide by 2 flip-flop |  |
| '#2Q  | Feedback for 2D, this pin is also cascaded to U1010 (divide by 12 counter) |  |

* **U1010: SN74LS92D (Divide-by-12)**
	+ Description: This component is divide-by-12 counter cascaded from divide-by-4 flip-flops. In order to generate 500kHz clock from 24MHz clock it has to be divided 48. However there were no such a single chip divider thus we cascaded divide-by-4 and 12. It has 2V of logic high minimum input voltage it is within output voltage level of divide-by-4 flip-flops, and it has high-level output voltage 2.4V (minimum) which is high enough to drive UXXXX (LTM4619). This divider outputs clock signal with duty ratio of 50%. Pull-down resistor on the pin QD pulls to logic low while starting up the board and it enable UXXXX (LTM4619) force continuous operation until UXXXX receive 500kHz clock signal.
	+ **U1010: SN74LS92D Pin Description**

| **Pin Name**  | **Description** |  |
| --- | --- | --- |
| CKB  | This pin is connected to QA in order to function as a divide by 12 counter. |  |
| CKA  | This is an input of divide by 12 counter. It is cascaded form divide by 4 flip-flops |  |
| QA  | Feedback to CKB according to the datasheet |  |
| QB  | Test Point (Not used) |  |
| QC  | Test Point (Not used) |  |
| QD  | Output of the divide by 12 counter (500kHz clock) with 100k ohms pull-down resister |  |
| R0(1)  | Connected to GND to enable divide by 12 counter |  |
| R0(2)  | Connected to GND to enable divide by 12 counter |  |

**Resistors**

* R1000: 11.5 kohm 0805, 1%, 1/8 W
	+ Description: 11.5 kohm feedback resistor which programs output voltage of Vout1 of UXXXX (LTM4619) to be 5V. See the equation and the table 1 of the datasheet of LTM4619.
* R1001: 19.1k ohms 0805, 1%, 1/8 W
	+ Description: 19.1k ohms feedback resistor which programs output voltage of Vout2 of UXXXX (LTM4619) to be 3.3V. See the equation and the table 1 of the datasheet of LTM4619.
* R1002: 0.06 ohm 0805, 1%, 1/8 W
	+ Description: This resistor adjust the circuit-breaker resistor's (Rcb) value. It is in series with the drain (hence RDS(on) of Q1000 to make up Rcb. The voltage drop across it is used to detect an overcurrent event given that it is greater than 300 mV. See Q1000 and U1001.
	+ Specifications/ Calculations: Over-current threshold was calculated assuming input voltage 10V, 90% efficiency and 1.5 of safety factor as follows. {2.2A\*3.3V/10V+0.5A\*(5V/10V)}\*(1.5/0.9)=1.62A Since circuit-breaker trip threshold voltage is 300mV, Rcb has to be 0.185 ohm. (300mV/1.62V=0.185 ohm) and typical value of RDS(on) of Q1000 is 0.125 ohm. R1002 is calculated as follows R1002=0.185-0.125=0.06ohm
	+ TODO: Value has to be verified
* R1003: 43k ohm 0805, 1%, 1/8 W, Cut Tape
Value unchanged from Capstone 2009 [LV2C:GFE:R2253]
	+ Description: R1003 along with Q1001 and Q1002 will "emulate" an overcurrent trigger event as seen by U1001 when an overvoltage at the SPS output trigger event as seen by U1002 or 1003 occurs. See Q1001 and Q1002. When the SPS +3.3 V or 5V output rises above a certain threshold, the output of U1002 or U1003 goes high, turning Q1001 or Q1002 on. When this happens it pulls pin 2 of U1002 or U1003 very close to ground and current flows through R1003 and Q1001 or Q1002. Now that pin 2 is close to ground and pin 1 is normally close to the power bus voltage this is much greater than 300 mV this causing an overcurrent trigger event for U1001. R1003 limits the extra current pulled through Q1001 and Q1002 when it is turned on.
	+ Specifications/ Calculations: In normal SPS operation, the voltage drop across Rcb will be less than 300 mV and R1003 is connected to the high impedance pin 2 of U1001 so no current flows through it. If there is an overvoltage trigger event at the SPS output, Q1001 or Q1002 or both are turned on conducting current through R1003 which will have a voltage drop of approximately 300 mV less than the power bus voltage: VR1003 = 16.8 V - 300 mV = 16.5 V. This results in a current boost of about IR1003 = 16.5 V / 47 kohm = 351 uA which is negligible.
* R1004: 100 kohm, 0805, 1%, 1/8W, Cut Tape, Value is unchanged from Capstone 2009 [LV2C:GFE:R2218] Rohm, MCR10EZHF1003 (Digi-Key p/n RHM100KCCT-ND $0.38/10) http://www.rohm.com/products/databook/r/pdf/mcr10.pdf.
	+ Description: R2218 provides a DC path from the SPS ground to chassis ground. See page 29 of the CAN Node Switch Mode Power Supply (SPS) (200) section in the Component Design for LV2 Power Electronics (Except Main Battery) engineering design notes.
* R1005: 19.1k ohm 0805, 1%, 1/8 W
	+ Description: This is TLV3012AIDBVT (U1002) overvoltage lockout resistor network (R1005, R1007) for SPS output +3.3V. This resistor along with R1007 works as a voltage divider for IN+ (pin3 of U1002) from +3.3 V SPS output rail, and set overvoltage lockout at 3.61V. Resistor value was calculated based on the equation along with figure3 of TLV3012AIDBVT datasheet. We arbitrary set value of R1007 to be 10k ohm to solve for R1005. Divided voltage from +3.3V supply is compared to internal reference voltage (1.242V) of U1002. Output (pin1 of U1002) becomes high when SPS+3.3V ramps up greater than 3.61V. See U1002 for more detail.
* R1006: 34k ohm 0805, 1%, 1/8 W
	+ Description: This is TLV3012AIDBVT (U1003) overvoltage lockout resistor network (R1006, R1008) for SPS output +5V. This resistor along with R1008 works as a voltage divider for IN+ (pin3 of U1003) from +5V SPS output rail, and set overvoltage lockout at 5.46V. Resistor value was calculated based on the equation along with figure3 of TLV3012AIDBVT datasheet. We arbitrary set value of R1008 to be 10k ohm to solve for R1006. Divided voltage from +5V supply is compared to internal reference voltage (1.242V) of U1003. Output (pin1 of U1003) becomes high when SPS+5V ramps up greater than 5.46V. See U1003 for more detail.
* R1007: 10k ohm 0805, 1%, 1/8 W
	+ Description: This is TLV3012AIDBVT (U1002) overvoltage lockout resistor network (R1005, R1007) for SPS output +3.3V. This resistor along with R1005 works as a voltage divider for IN+ (pin3 of U1002) from +3.3 V SPS output rail, and set overvoltage lockout at 3.61V. Resistor value was chosen arbitrary to solve for the resistor value of R1005 using the equation along with figure3 of TLV3012AIDBVT datasheet. Divided voltage from +3.3V supply is compared to internal reference voltage (1.242V) of U1002. Output (pin1 of U1002) becomes high when SPS+3.3V ramps up greater than 3.61V. See U1002 for more detail.
* R1008: 10k ohm, 0805, 1%, 1/8 W
	+ Description: This is TLV3012AIDBVT (U1003) overvoltage lockout resistor network (R1006, R1008) for SPS output +5V. This resistor along with R1006 works as a voltage divider for IN+ (pin3 of U1003) from +5V SPS output rail, and set overvoltage lockout at 5.46V. Resistor value was chosen arbitrary to solve for the resistor value of R1006 using the equation along with figure3 of TLV3012AIDBVT datasheet. Divided voltage from +5V supply is compared to internal reference voltage (1.242V) of U1003. Output (pin1 of U1003) becomes high when SPS+5V ramps up greater than 5.46V. See U1003 for more detail.
* R1026:
	+ Description: 100k ohm pull-down resistor. This resistor pulls Mode/PLLIN pin of UXXXX (LTM4619) to ground while it is starting up. Logic low on this pin enables force continuous operation, and UXXXX operate at switching frequency of 780 kHz until 500 kHz external clock signal from TQM5200 becomes available.
* R1103 61.9 kohm, 0805, 1%, 1/8 W, Cut Tape
Value unchanged from Capstone 2009 [LV2C:GFE:R2250]
	+ Description: R1103 is part of the UVLO resistor divider of U1001.
	+ Specifications/ Calculations: The UVLO voltage was specified to be 9 V. See page 8 and Figure 3 in the MAX5902 datasheet. Letting R1104 = 10.0 kohm and using the typical value of Von/!off = 1.26 V, the UVLO formula from page 8 in the datasheet is R1103 = R1104 \* ((VUVLO / (Von/!off)) - 1) = 61.4 kohm. The closet standard value was 61.9 kohm.
* R1104: 10 kohm, 0805, 1%, 1/8 W, Cut Tape
Value is unchanged from Capstone 2009 [LV2C:GFE:R2251]
	+ Description: This resistor is one of the UVLO resistor divider of U1001. It set UVLO threshold at 9V.
	+ Justification: This value is arbitrarily chosen.

**Capacitors**

* C1000:
	+ Description: 22pF capacitor between Vout1 and Vfb1 of UXXXX (LTM4619). Value of this capacitor was chosen from typical application in the datasheet.
* C1001:
	+ Description: Output capacitor of UXXXX (LTM4619). Value was chosen from datasheet.
* C1002: 0.2nF
	+ Description: This capacitor programs soft-start time of Vout1 of UXXX. 0.2nF was chosen to set soft-start time to be 123us.
* C1003:
	+ Description: Input capacitor of UXXXX (LTM4619) 10uF of minimum capacitance in the datasheet was chosen and it’s decoupled with identical capacitor C1004.
* C1004:
	+ Description: Input capacitor of UXXXX (LTM4619) 10uF of minimum capacitance in the datasheet was chosen and it’s decoupled with identical capacitor C1003.
* C1005: Node Power Supply Filter Capacitor Value unchanged from Capstone 2009 [LV2C:GFE:C2206] Part Description: 22 uF, 25 V, Tant, T491 Series, 7343-31 (EIA), Cut Tape, RoHS Compliant???, Kemet, T491D226K025AT (Digi-Key p/n 399-3782-1-ND $0.65/1) http://www.kemet.com/kemet/web/homepage/kechome.nsf/vapubfiles/F3102T491.pdf/$file/F3102T491.pdf.
	+ Description: C1005 acts as a noise filter between the power bus and SPS. It also serves as a local energy storage node.
	+ Specifications/ Calculations: It needs to have a voltage rating greater than 20 V and a low equivalent series resistance (ESR) thus a tantalum capacitor was chosen due to their low ESR at a higher capacitance. TODO: Voltage rating is a bit low.
* C1006: Value unchanged from Capstone 2009 [LV2C:GFE:C2207] Part Description: 0.33 uF, 50 V, 0805, X7R, Cut Tape, RoHS Compliant, Murata Electronics North America , GRM219R71H334KA88D (Digi-Key p/n 490-3327-1-ND $3.09/10) http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/GRM219R71H334KA88.pdf.
	+ Description: C1006 is a high frequency noise filter between the power bus and SPS. It did not have to have as high a capacitance as C1005 so the trade off was to get a lower value at a low ESR. \*Specifications/ Calculations: It needs to have a voltage rating greater than 20 V and the capacitance value was not very critical but should be much lower than C1005.
* C1007:
	+ Description: 22pF capacitor between Vout2 and Vfb2 of UXXXX (LTM4619). Value of this capacitor was chosen from typical application in the datasheet.
* C1008: 100uF Output capacitor of UXXXX (LTM4619).
Value was chosen from datasheet.
* C1009: 0.2nF
	+ Description: This capacitor programs soft-start time of Vout2 of UXXX. 0.2nF was chosen to set soft-start time to be 123us.
* C1010: 2.7 uF, 10 V, 0805, X5R, Cut Tape, RoHS Compliant, Kemet
C0805C275K8PACTU (Digi-Key p/n 399-3127-1-ND $7.02/10)
Value is unchanged from Capstone2009 [LV2C:GFE:C1010]
	+ Description: This is a TLV3012AIDBVT "Secondary Power Supply" Cap (C1010). This capacitor prevent U1002 from power cycling by acting like an instant power supply for U1002 when SPS-output drops down by certain level.
	+ Justification: 2.7uF capacitor ensures U1002 powered more than 0.5s when SPS-output drops by 1V. See Capstone 2009 [LV2C:GFE:C1010] for more detail.
* C1011: 15 nF TLV3012AIDBVT Overvoltage Detection Cap
Value is unchanged from Capstone 2009 [LV2C:GFE:C2251] Part Description: 0.015 uF, 100 V, 0805, X7R, Cut Tape, RoHS Compliant, AVX Corporation, 08051C153KAT2A (Digi-Key p/n 478-1359-1-ND $2.64/10)
See [LV2C:GFE:C2251] for more detail.
* C1012:2.7 uF, 10 V, 0805, X5R, Cut Tape, TLV3012AIDBVT "Secondary Power Supply" Cap (C1010)
RoHS Compliant, Kemet, C0805C275K8PACTU (Digi-Key p/n 399-3127-1-ND $7.02/10) http://www.kemet.com/kemet/web/homepage/kechome.nsf/vapubfiles/F3102X5R.pdf/$file/F3102X5R.pdf.
	+ Description: This capacitor prevent U1003 from power cycling by acting like an instant power supply for U1003. Value is the same as corresponding capacitor in [Capstone2009 LV2C:GFE:C2250]
* C1013: 15 nF TLV3012AIDBVT Overvoltage Detection Cap
Value is unchanged from Capstone 2009 [LV2C:GFE:C2251] Part Description: 0.015 uF, 100 V, 0805, X7R, Cut Tape, RoHS Compliant, AVX Corporation, 08051C153KAT2A (Digi-Key p/n 478-1359-1-ND $2.64/10) http://rocky.Digi-Key.com/WebLib/AVX/Web%20Data/X7R%20(C).pdf.
See [LV2C:GFE:C2251] for more detail.
* C1031: 100nF Noise filtering capacitor for U1009(Dflip-flops)
* C1032: 100nF Noise filtering capacitor for U1010(divide by 12)

**Others**

* L1000: Power Bus input Choke
Part Description: CMS2-4-R Common Mode Inductors 102 uH, Micro-PAC Plus Package, RoHS Compliant, Cut Tape, (Digi-Key p/n: 513-1115-1-ND, $3.37/1).
	+ Description: : Common mode choke (balanced inductor). It is used as an EMI filter between the power bus and the SPS.
	+ Specifications/ Calculations: The capstone 2006 value was chosen through a trial and error process from the previous LV2 SPS design. Each inductor of the choke is 100 uH. See page 13 of the CAN Node Switch Mode Power Supply (SPS) (200) section in the Component Design for LV2 Power Electronics (Except Main Battery) engineering design notes \*Note: (CMS1-11-R) has gone non-stock at Digi-Key and replacements are available in lots of 2000. New suggested part(CMS1-7-R) is dissimilar in value, but same physical size.
* F1000: Node Power Supply Fuse
2000 mA, 63 V, 1206, Fast Acting Short Time Lag, RoHS Compliant, TYCO Electronics, 1206SFF200F/63-2 (Digi-Key p/n 1206SFF200F/63CT-ND $0.46/1) http://documents.tycoelectronics.com/commerce/DocumentDelivery/DDEController?Action=srchrtrv&DocNm=SCD25801&DocType=CD&DocLang=EN
	+ Description: This fuse protects the SPS from currents greater than 2000 mA. Its direct purpose however is to protect the power bus from a short circuit fault on the SPS side.
	+ Specifications/ Calculations: Since the specified maximum SPS current is 2000 mA we chose a fuse rated at 2000 mA. The opening time for the fuse according to its datasheet is .05 s at a current of 8 A, or 5 s at 5 A. Currents of 2 A or below are 4 hours minimum, therefore this fuse will only protect the SPS or power bus from gross currents due to some fault on either side (power bus or SPS) and not to keep the SPS output current within spec, that is U1001's job.
	+ TODO: verify current rating
* TVS1000: the same part from capstone 2009 [LV2C:GFE:TVS2201] was used.
18 V, SMB, Unidirectional, Cut Tape, RoHS Non-Compliant, Diodes Inc, SMBJ18A-13 (Digi-Key p/n SMBJ18ADICT-ND $0.89/1) http://www.diodes.com/datasheets/ds19002.pdf.
	+ Description: A transient voltage suppressor (TVS), this "zener like" diode protects the SPS in the event of an overvoltage at the input. \*Specifications/ Calculations: It should have a breakdown voltage of about 20 V (unlikely maximum bus voltage) and a current carrying capacity greater than the fuse rated current. It should have a fast response time and be unidirectional. In the event of a sustained overvoltage at the input the only allowable part which can be destroyed is the fuse, F1000. That is what we want. \*Note: . The original capstone2006 part is no longer available in Digi-Key. Re-specify or find new vendor. One suggested replacement is B72500D200A60V7 (Digi-Key p/n: 495-3413-1-ND $0.20/1) http://www.epcos.com/inf/75/ds/cd\_standard.pdf This is a simple Zener type ESD suppressor in an 0603 package.
	Another replacement possibility is: V2F118C400Y1FDP, Digi-Key p/n:478-2486-1-ND. The difficulty here is that new replacement doesn't handle the current that we are looking for, it maxes out at 1A and would blow before the fuse.
	A final possibility, as the LT3907 is capable of withstanding up to 62V, it could be argued to simply not populate this part, though some ESD protection would be nice.
* Q1000: The same part from capstone 2009 [LV2C:GFE:Q2250] was Selected
-60 V, -3 A, SOT-23-6, P-Channel MOSFET, Cut Tape, RoHS Compliant, Zetex Inc, ZXMP6A17E6TA (Digi-Key p/n ZXMP6A17E6CT-ND $0.75/1)
	+ Description: This PMOS works as circuit breaker controlled by U1001. RDS(on) of saturated Q1000 is used by U1001 to sense current flowing on power line. See capstone 2009 [LV2C:GFE:Q2250]
* Q1001: The same part from capstone 2009 [LV2C:GFE:Q2251] was Selected
100 V, 170 mA, RDS(on) = 10 ohm @ Vgs = 4.5V, SOT-23, Cut Tape, RoHS Compliant???, N-Channel Logic-Level MOSFET, Infineon Technologies, BSS123E6327 (Digi-Key p/n BSS123INCT-ND $0.36/1) http://rocky.Digi-Key.com/WebLib/Infineon/Web%20Data/BSS123.pdf.
	+ Description: • This Mosfet is off under normal operation, but in the event SPS-5V output exceeds 5.46V, it is turned on by U1002 (comparator sensing overvoltage). Then pin2 (Drain) of U1001 becomes almost ground, and Q1000 shut off current.
* Q1002: The same part from capstone 2009 [LV2C:GFE:Q2251] was Selected
100 V, 170 mA, RDS(on) = 10 ohm @ Vgs = 4.5V, SOT-23, Cut Tape, RoHS Compliant???, N-Channel Logic-Level MOSFET, Infineon Technologies, BSS123E6327 (Digi-Key p/n BSS123INCT-ND $0.36/1) http://rocky.Digi-Key.com/WebLib/Infineon/Web%20Data/BSS123.pdf.
	+ Description: This Mosfet is off under normal operation, but in the event SPS-3.3V output exceeds 3.6V, it is turned on by U1002 (comparator sensing overvoltage). Then pin2 (Drain) of U1001 becomes almost ground, and Q1000 shut off current.
* CR1000: TLV3012AIDBVT "Secondary Power Supply" Schottky Diode
The same part with capstone 2009 [LV2C:GFE:CR2250] was selected
30 V, 1.5 A, 4 ns, New MiniPower 2P, Cut Tape, RoHS Compliant???, Panasonic - SSG, MA2Q70500L (Digi-Key p/n MA2Q70500LCT-ND $0.83/1)
* CR1001: TLV3012AIDBVT "Secondary Power Supply" Schottky Diode
The same part with capstone 2009 [LV2C:GFE:CR2250] was selected
30 V, 1.5 A, 4 ns, New MiniPower 2P, Cut Tape, RoHS Compliant???, Panasonic - SSG, MA2Q70500L (Digi-Key p/n MA2Q70500LCT-ND $0.83/1)

References

* + 1. TQM5200 Hardware Manual: <http://psas.pdx.edu/avionics/capstone2010/design/tqm5200/TQM5200.HWM.204.pdf>
		2. MPC5200 User Manual: <http://psas.pdx.edu/avionics/capstone2010/design/tqm5200/MPC5200UM.pdf>