Preliminary

MOPS/520

Technical Manual

Rev. 1.0

JUMP*tec*®
Industrielle Computertechnik AG
Brunnwiesenstraße 16
94469 Deggendorf/ Germany

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2. USER INFORMATION

In this document JUMP*tec*® **Industrielle Computertechnik AG will also be referred to by the short form "**JUMP*tec*®**".**

The information in this document has been carefully checked and is believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies. Furthermore, JUMP*tec*® **reserves the right to make changes to any portion of this manual to improve reliability, function or design.** JUMP*tec*® **does not assume any liability for any product or circuit described herein.**

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2.2 General

For the circuits, descriptions and tables indicated no responsibility is assumed as far as patents or other rights of third parties are concerned.
The information in the Technical Descriptions describes the type of the boards and shall not be considered as assured characteristics.

2.3 Warranty

Each board is tested carefully and thoroughly before being shipped. If, however, problems should occur during the operation, please check your user specific settings of all boards included in your system. This is often the source of the fault. If a board is defective, it can be sent to your supplier for repair. Please take care of the following steps:

1. **The board returned should have the factory default settings since a test is only possible with these settings.**
2. **In order to repair your board as fast as possible we require some additional information from you. Please fill out the attached Repair Form and include it with the defective board.**
3. **If possible the board will be upgraded to the latest version without additional cost.**
4. **Upon receipt of the board please be aware that your user specific settings were changed during the test.**

Within the warranty period the repair is free of charge as long as the warranty conditions are observed. Because of the high test expenditure you will be charged with the test cost if no fault is found. Repair after the warranty period will be charged.

This JUMP*tec*® product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period JUMP*tec*® will at its option either repair or replace defective products.

For warranty service or repair the product must be returned to a service facility designated by JUMP*tec*®.

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance or handling by buyer, unauthorized modification or misuse, operation outside of the product´s environmental specifications or improper installation or maintenance.

JUMP*tec*® will not be responsible for any defects or damages to other products not supplied by JUMP*tec*® that are caused by a faulty JUMP*tec*® product.

2.4 Support, problems and failure analysis

It is not in the responsibility of JUMP*tec*® to supply you with informations about standard PC technology. Please find a selection of different information sources for your convenience in chapter „Literature“

Before contacting JUMP*tec*® please check first our web page for available information (newest manuals, application notes etc.). If you can't solve the problem on your own with this documents, do not hesitate to contact us by email or phone. Please prepare yourself to answer a few questions like

- **which JUMP*tec*® module(s) is(are) concerned?**
- **what serial numbers (xx???????)?**
- **what BIOS versions?**
- **since when is this problem known**
- **is this problem already reported (to whom?)**
- **and so on...**

Note: You can save time and increase the problems solving process by using the FAReq.DOT form from our web page www.jumptec.de for problem reports.

3. INTRODUCTION

The *MOPS/520* is based on the ÉlanSC520 microcontroller (32-bit Am5x86® CPU). It integrates the complete functionality of motherboard with CPU, System-BIOS, up to 64 MByte SDRAM, keyboard-controller, real time clock and additional peripheral functions like COM1..COM4, LPT1, Floppy-interface, IDE-harddisk-interface, Watchdog, Ethernet access and optional CAN-Bus interface. The system runs with CPU clock speed 133MHz.

4. FEATURES

- Processor

  32-bit Am5x86® CPU (AMD ÉlanSC520) with 16 kByte write-back-Cache or

- Power Supply

  5V only supply

- Memory

  16/32/64MB SDRAM (onboard)

- Ethernet 10/100BaseT (Twisted Pair)

- Four serial ports, (COM1..COM4)

  Three standard RS232C serial ports with FIFO, 16550 compatible (COM1..COM3)

  COM4 is only TTL

- Parallel port, LPT1

  With ECP/EPP-support

- Floppy-interface

- Hard disk-interface

  IDE port up to 2 IDE Devices
  supports JUMPtec CHIPdisk

- Watchdog

- 256 KByte FLASH-BIOS (Phoenix)

- Real Time Clock

  With external Battery-support

- Keyboard Controller

- CAN-Bus Interface with INTEL® 82527 Controller

5. LIMITATIONS

Parallel Port
Due to chipset limitations parallel port mode ECP as well as parallel port base address 3BCh (in any mode) cannot be used when a PCI video adapter is installed on the system.
With ISA video adapters these restrictions do not apply.

Serial Ports
The SC520 integrated serial ports (serial port C and D on the MOPS/520) show two deviations from the standard UART behaviour:

The delta ring indicator bit in the modem status register (bit 2) is only set when the ring indicator signal has changed from an active to an inactive state since the last time the modem status register was read.
Usually this bit is set for RI changes from inactive to active as well.

In 16550 compatible mode a received data interrupt is generated when the very first data byte of a continuous data stream is placed in FIFO. This error only occurs for the first character of a continuous data stream received by the UART. Following the FIFO time-out interrupt for the first character received, the remainder of the data stream will be indicated according to the trigger value set in the RFRT bits of the UART FIFO control registers.

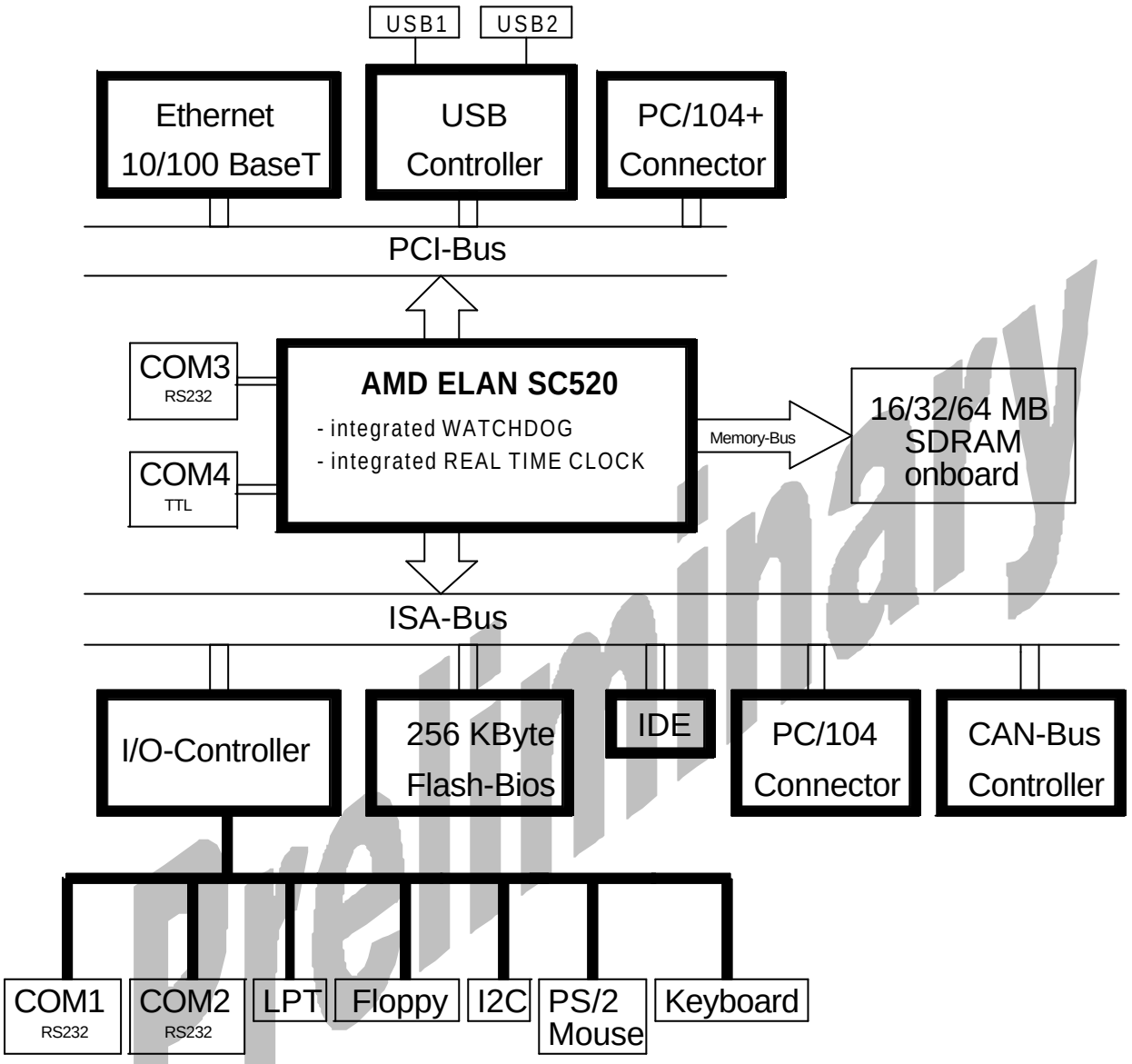
I/O Address Mapping
Only I/O addresses below 400h are mapped to the external ISA respectively PC104 bus. All higher I/O addresses are directed to PCI.

6. I/O MAP

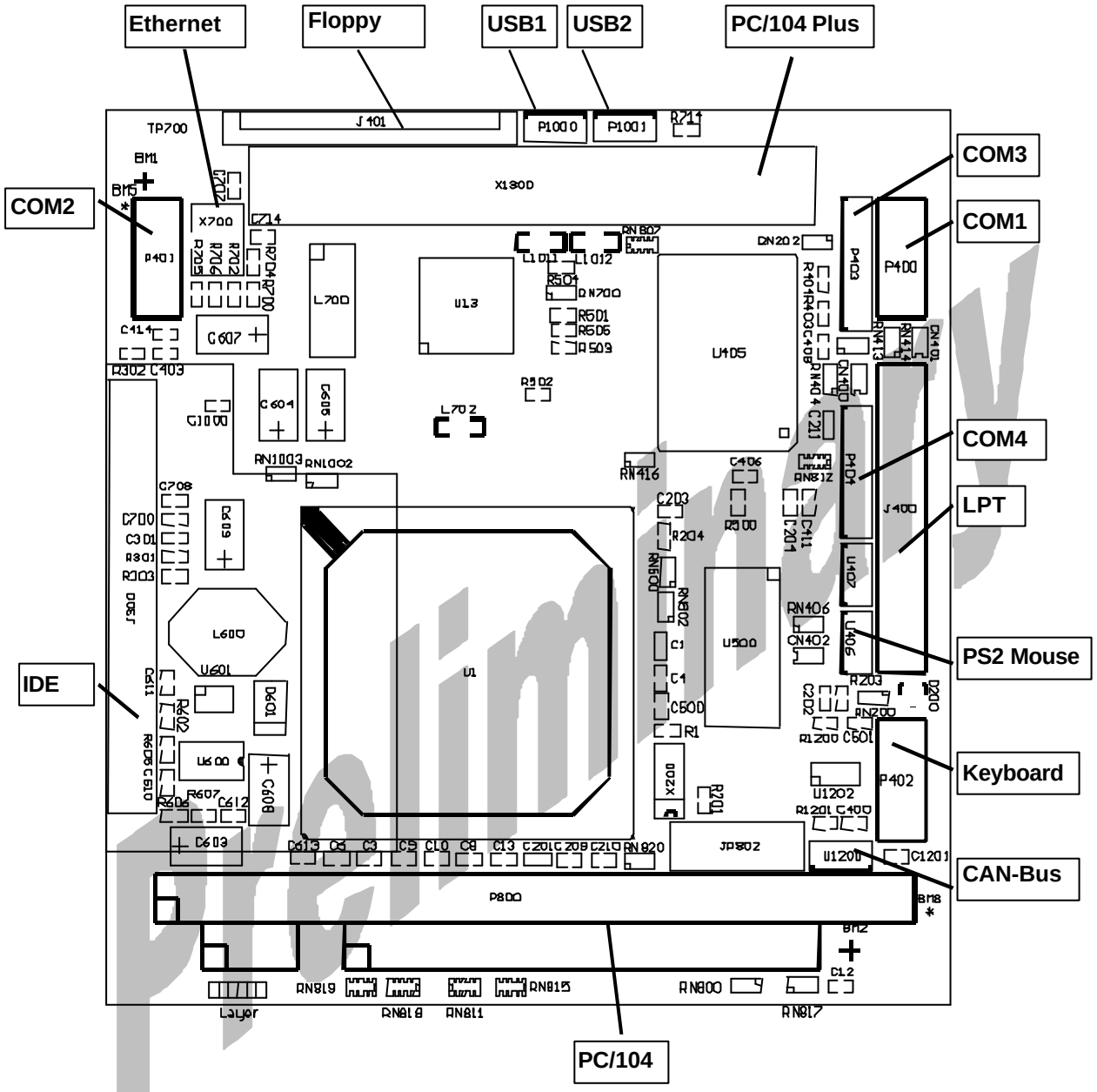
The I/O-port addresses of the processor module *MOPS/520* are functionally identical with a standard PC/AT.

I/O Addresses	MOPS/520 - onboard	Function
0000 - 001F	X	DMA-Controller 1
0020 - 003F	X	Interrupt-Controller 1
0040 - 0043	X	Timer
0050 - 005F		Onboard Control Registers
0060 - 0064	X	Keyboard-controller
0061	X	Port B Register
0070	X	NMI Enable Register
0070 - 0071	X	Real Time Clock
0080 - 008F	X	DMA Page Register 74LS612
0092	X	Port A Register (Fast A20 Gate)
00A0 - 00BF	X	Interrupt-Controller 2
00C0 - 00DF	X	DMA-Controller 2
00F0 - 00FF	X	Math-Coprocessor
0100 – 10F	X	Onboard Control Registers
01F0 - 01F8	X	Fixed Disk
0200 – 0207		Game I/O
020C-020D		Reserved
021F		Reserved
0274		Control Register 1 External SSD (Board 0 - 3)
0275		Control Register 1 External SSD (Board 4 - 7)
0278 – 027F		Parallel Port 2
02B0 - 02DF		Alternate Enhanced Graphics Adapter
02E1		GPIB (adapter 0)
02E2 - 02E3		Data acquisition (Adapter 0)
02E8 - 02EF	X	Serial Port 4
02F8 - 02FF	X	Serial Port 2
0300 – 030F		Onboard Network (default configuration)
0310 – 031F		Prototype Card
0360 – 0363		PC Network (low Address)
0364 – 0367		Reserved
0368 – 036B		PC Network (high Address)
036C – 036F		Reserved
0370 – 0377		Secondary Diskette Contoller
0378 – 037F	X	Parallel Port 1
0380 – 038F		SDLC, Bisynchronous 2
0390 – 0393		Cluster
03A0 - 03AF		Bisynchronous 1
03B0 - 03BF		Monochrom Disp. and Printer Adap.
03C0 - 03CF		Enhanced Graphic Adapter
03D0 - 03DF		Color/Graphic Monitor Adapter
03E8 - 03EF	X	Serial Port 3
03F0 - 03F7	X	Primary Diskette Controller
03F8 - 03FF	X	Serial Port 1

7. BLOCK DIAGRAM



8. CONNECTOR ARRANGEMENT



9. BIOS-DESCRIPTION

The *MOPS/520* is equipped with a Phoenix BIOS which is located in a Flash EPROM onboard. This device has 8bit wide access. Faster access (16bit) is provided by the shadow RAM feature (default).

9.1 The Setup Guide

With the PhoenixBIOS Setup programm, you can modify BIOS settings and control the special features of the computer. The setup programm uses a number of menus for making changes and turning the special features on or off.

General Information

To start the PhoenixBIOS setup utility press <F2> when the string Press <F2> to enter Setup is displayed during bootup. The Main Menu will be displayed.

The Menu Bar

The Menu Bar at the top of the window lists all the different menus. Use the left/right arrows to make a selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selection or exit the current menu. The table below describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	**General help window**
<Esc>	**Exit this menu**
¬ or ® Arrow key	**Select a different menu**
- or ¯ Arrow key	**Move cursor up and down**
<Tap> or <Shift-Tap>	**Cycle cursor up and down**
<Home> or <End>	**Move cursor to top or bottom of current window**
<PgUp> or <PgDn>	**Move cursor to next or previous page**
<F5> or <->	**Select the previous value for the current field**
<F6> or <+> or <Space>	**Select the next value for the current field**
<F9>	**Load default configuration values for this menu**
<F10>	**Save and Exit**
<Enter>	**Execute command or select submenu**
<Alt-R>	**Refresh screen**

To select an item**, simply use the arrow key to move the cursor to the field you want. Then use the plus and minus keys to select a value for that field. The Save Value commands in the Exit Menu save the values currently displayed in all the menus.**

To display a sup menu**, use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A pointer (▸) marks all sub menus.**

The Field Help Window

The help window on the right side of each menu displays the help text for the currntly selected field. It updates as you move the cursor to each field.

The General Help Window

Pressing <F1> or <Alt-F1> on any menu brings up the General Help Window that describes the legend keys and their alternates. Press <Esc> to exit the General Help Window.

The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Option	Description
System Time	**HH:MM:SS**	**Set the system time. Use <Enter to move to MM or SS.**
System Date	**MM/DD/YYYY**	**Set the system date. . Use <Enter to move to DD or YYYY.**
Legacy Diskette A	**360 kB, 5 ¼ "** **1.2 MB, 5 ¼ "** **720 kB, 3 ½ "** 1.44/1.25 MB, 3 ½ " **2.88 MB, 3 ½ "** **Not Installed** **Disabled**	**Select the type of floppy disk drive installed in the system.**
‣ **Primary Master**	**autodetected drive**	**Displays result of PM autotyping.**
‣ **Primary Slave**	**autodetected drive**	**Displays result of PS autotyping.**
‣ **Memory Shadow**	**sub menu**	**Opens Memory Shadow Menu**
System Memory	**N/A**	**Displays amount of conventional memory detected during bootup.**
Extended Memory	**N/A**	**Displays amount of extendedmemory detected during bootup.**

Selecting one of the Master or Slave sub menus displays a menu like this:

Feature	Option	Description
Type	**None** **User** Auto **CD-ROM**	**None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed.** **User = End user supplies the hdd information.** **Auto = Autotyping, the drive itself supplies the information.** **CD-ROM = CD-ROM drive.**
Cylinders	**1 to 65,536**	**Number of cylinders.**
Heads	**1 to 256**	**Number of read/write heads.**
Sectors	**1 to 63**	**Number of sectors per track.**
Maximum Capacity (CHS)	**N/A**	**Displays the calculated size of the drive in CHS**
Total Sectors*	**N/A**	**Total number of sectors in LBA mode**
Maximum Capacity (LBA)*	**N/A**	**Displays the calculated size of the drive in LBA**
Multi-Sector Transfer	**Disabled** **Standard** **2 sectors** **4 sectors** **8 sectors** 16 sectors	**Any selection except Disabled determines the number of sectors transferred per block.** **Standard is 1 sector per block.**
LBA Mode Control	**Disabled** Enabled	**Enabling LBA causes Logical Block Addressing to be used in place of CHS.**

***Only if LBA Mode Control enabled**

Memory Shadow sub menu:

Feature	Option	Description
Video Shadow	**Disabled** Enabled	**Enables/disables shadowing of video ROM**
C800 – CFFF	Disabled **Enabled**	**Accesses to this upper memory region go to the ISA bus if Disabled or to local memory if Enabled.** **NOTE: This option is not displayed if VGA BIOS exceeds 32kB! In that case this region is shadowed automatically.**
D000 – D7FF	Disabled **Enabled**	**see above.**
D800 – DFFF	Disabled **Enabled**	**see above.**

The Advanced Menu

Selecting „Advanced“ from the menu bar displays this menu:

Feature	Option	Description
▸ **Advanced Chipset Control**	**sub menu**	**Opens Advanced Chipset Control sub menu.**
▸ **PCI Configuration**	**sub menu**	**Opens PCI Advanced sub menu.**
PNP OS installed	**Yes** No	**If your system has a PNP OS (e.g. Win95) select Yes to let the OS configure PNP devices not required for boot. No makes the BIOS configure them.**
Reset Configuration Data	No **Yes**	**Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.**
PS/2 Mouse	**Disabled** **Enabled** Auto	**PS/2 mouse configuration.**
▸ **Keyboard Features**	**sub menu**	**Opens Keyboard Features sub menu.**
▸ **I/O Device Configuration**	**sub menu**	**Opens I/O Device Configuration sub menu.**
Large Disk Access Mode	DOS **Other**	**Select DOS if you have DOS. Select Other if you have another OS such as UNIX.** **A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.**
Halt On Errors	**Yes** No	**Determines if post errors cause the system to halt.**

Advanced Chipset Control sub menu:

Feature	Option	Description
CPU Speed	**100 MHz** 133 MHz	**Select CPU frequency.**
Cache Mode	Write Back **Write Through**	**Select SC520 L1 cache mode.**
CAS latency	3T **2T**	**Select CAS latency.**
RAS to CAS delay	**2T** 3T **4T**	**Select RAS to CAS delay.**
RAS Precharge time	**2T** 3T **4T** **6T**	**Select RAS precharge time.**
Refresh cycle time	**7.8 us** 15.6 us **31.2 us** **62.5 us**	**Select SDRAM refresh cycle time.**
SDRAM buffer	**Disabled** Enabled	**The integrated SDRAM read/write buffer increases overall system performance.**
ISA bus cycle duration:	**400ns** 800ns **1.2us** **2us**	**Set the duration of a complete ISA bus cycle.**

PCI Configuration sub menu:

Feature	Option	Description
▸ **PCI Device, Slot #1**	**sub menu**	**Opens sub menu to configure slot 1 PCI device**
▸ **PCI Device, Slot #2**	**sub menu**	**Opens sub menu to configure slot 2 PCI device**
▸ **PCI Device, Slot #3**	**sub menu**	**Opens sub menu to configure slot 3 PCI device**
▸ **PCI Device, Slot #4**	**sub menu**	**Opens sub menu to configure slot 4 PCI device**
PCI IRQ line 1	**Disabled** Auto Select **IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15**	**Select IRQ for PIC interrupt INTA. Select Auto to let the BIOS assign the IRQ.**
PCI IRQ line 2	**see above**	**Select IRQ for PIC interrupt INTB. Select Auto to let the BIOS assign the IRQ.**
PCI IRQ line 3	**see above**	**Select IRQ for PIC interrupt INTC. Select Auto to let the BIOS assign the IRQ.**
PCI IRQ line 4	**see above**	**Select IRQ for PIC interrupt INTD. Select Auto to let the BIOS assign the IRQ.**
▸ **PCI/PNP ISA UMB Region Exclusion**	**sub menu**	**Opens UMB Region Exclusion sub menu.**
▸ **PCI/PNP ISA IRQ Resource Exclusion**	**sub menu**	**Opens IRQ Exclusion sub menu.**
Assign IRQ to PCI VGA	Yes **No**	**Actually most graphic cards do not need an IRQ assigned, but Win98 2nd Edition doesn't work correctly if no IRQ is assigned**

PCI Device, Slot #X sub menu:

Feature	Option	Description
Option ROM Scan	**Disabled** Enabled	**Initialize device expansion ROM**
Enable Master	**Disabled** Enabled	**Enables device in slot as a PCI bus master. Not every device can function as a master. Check your device documentation.**
Latency Timer	**20h,** 40h**, 60h, 80h, A0h, C0h, E0h**	**Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.**

PCI/PNP ISA UMB Region Exclusion sub menu:

Feature	Option	Description
C800 - CBFF	Available **Reserved**	**Reserves the specified block of upper memory for use by legacy ISA devices.**
CC00 - CFFF	**see above**	**see above**
D000 – D3FF	**see above**	**see above**
D400 – D7FF	**see above**	**see above**
D800 - DBFF	**see above**	**see above**
DC00 - DFFF	**see above**	**see above**

PCI/PNP ISA IRQ Exclusion sub menu:

Feature	Option	Description
IRQ3	Available **Reserved**	**Reserves the specified IRQ for use by legacy ISA devices.**
IRQ4	**see above**	**see above**
IRQ5	**see above**	**see above**
IRQ7	**see above**	**see above**
IRQ9	**see above**	**see above**
IRQ10	**see above**	**see above**
IRQ11	**see above**	**see above**
IRQ14 (only visible if IDE disabled)	**see above**	**see above**
IRQ15	**see above**	**see above**

Keyboard Features sub menu:

Feature	Option	Description
Numlock	Auto **On** **Off**	**On or Off turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric key pad.**
Key Click	Disabled **Enabled**	**Turns audible key click on.**
Keyboard auto-repeat rate	30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec**	**Sets the number of times to repeat a keystroke per second if you hold the key down.**
Keyboard auto-repeat delay	**¼ sec,** ½ sec**, ¾ sec, 1 sec**	**Sets the delay time after the key is held down before it begins to repeat the keystroke.**

I/O Device Configuration sub menu:

Feature	Option	Description
Local Bus IDE Adapter:	**Disabled** Enabled	**Enables onboard IDE device.**
Floppy disk controller	**Disabled** Enabled **Auto**	**Enables onboard FDC controller.**
Base I/O address	Primary **Secondary**	**Selects base address of onboard FDC conroller. (Primary = 3F0h, Secondary = 370)**
Serial port A **Serial port B**	**Disabled** Enabled **Auto** **OS Controlled**	**Disabled turns off the port.** **Enabled requires end user to enter the base I/O address and the IRQ.** **Auto makes the BIOS configure the port.** **OS Controlled lets the PNP OS configure the port after bootup.**
Base I/O address	**3F8h, 2F8h, 3E8h, 2E8h**	**Select I/O base of port A and B.**
IRQ	**IRQ 3, IRQ 4, IRQ 10 (only port A), IRQ 11 (only port B)**	**Select IRQ of port A and B.**
Serial port C **Serial port D**	Disabled **Enabled**	**Disabled turns off the port.** **Enabled sets port C to IRQ 4, address 3f8h and port D to IRQ3, address 2f8.**
Parallel Port	**Disabled** **Enabled** Auto **OS Controlled**	**Disabled turns off the port.** **Enabled requires end user to enter the base I/O address and the IRQ.** **Auto makes the BIOS configure the port.** **OS Controlled lets the PNP OS configure the port after bootup.**
Mode	**Output only** Bi-directional **ECP** **EPP**	**Set the mode for the parallel port.**
Base I/O address	**378h, 278h, 3BCh**	**Select I/O base of port.**
IRQ	**IRQ 5, IRQ 7**	**Select IRQ of parallel port.**
DMA	**DMA 1, 3**	**Select DMA channel of port if in ECP mode.**
‣ Watchdog Settings	**sub menu**	**Opens Watchdog Settings sub menu**
Onboard CAN controller:	**Disabled** Enabled **Auto** **OS Controlled**	**Disabled turns off the onboard CAN controller.** **Enabled requires end user to enter the base I/O address and the IRQ.** **Auto makes the BIOS configure the controller.** **OS Controlled lets the PNP OS configure the controller after bootup.**
Base I/O address	**400, 1000, 1600,** 2000	**Set the base I/O address of the onboard CAN controller (range = 256 Byte).**
IRQ	5**, 9**	**Select the interrupt for the onboard CAN controller.**
Onboard ethernet controller:	**Disabled** Enabled	**Enable /disable the onboard PCI ethernet controller.**

Watchdog Settings sub menu:

Feature	Option	Description
Mode	Disabled **Reset** **NMI**	**Select watchdog operation mode.**
Delay	**No Delay** **0.5s, 1s,** 2s**, 4s, 8s, 16s, 32s**	**The time until the watchdog counter starts counting. Useful to handle longer boot times.**
Timeout	**0.5s, 1s, 2s,** 4s**, 8s, 16s, 32s**	**Max. trigger periode.**

The Security Menu

Selecting „Security“ from the menu bar displays this menu:

Feature	Option	Description
Set User Password	**Up to seven alphanumeric characters**	**Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.**
Set Supervisor Passord	**Up to seven alphanumeric characters**	**Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.**
Password on boot	Disabled **Enabled**	**Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabed, BIOS assumes user is booting.**
Diskette access	**User** Supervisor	**Enabled requires supervisor password to access floppy disk.**
Virus check reminder **System backup reminder**	Disabled **Daily** **Weekly** **Monthly**	**Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with „Y“. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and Monthly on the first boot of the month.**

Enabling „Supervisor Password“ requires a password for entering Setup.
The passwords are not case sensitive**!**

Note: User and Supervisor passwords are related! You cannot have a User password without first creating a Supervisor password.

The Boot Menu

See chapter „Boot Utilities“ below

The Exit Menu

The following sections describe the five possible options of the Exit Menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu to exit.

Exit Saving Changes

Saves all the selections and exits setup. The next time you boots, the BIOS configures the system according to the Setup selection stored in CMOS.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

Select to display the default values for all the Setup menus.

Discard Changes

If, during a Setup session, you changeyour mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Save Changes

Saves all the selection without exiting Setup. You can return to the other menus if you want to review and change your selection.

9.2 Boot Utilities

QuietBoot

Rigth after you turn on or reset the computer, Quietboot displays a graphical logo instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:
- **You press <Esc> to display the POST screen**
- **You press <F2> to enter Setup**
- **POST issues an error message**
- **The BIOS or an option ROM requests keyboard input**

MultiBoot

MultiBoot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CD-ROM or network card. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in The Boot First Menu**.**

MultiBoot consists of 4 menus:

The Setup Boot Menu

Feature	Option	Description
Floppy Check	Disabled **Enabled**	**Enabled verifies floppy type on boot; disabled speeds boot.**
Summary Screen	Disabled **Enabled**	**If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.**
QuickBoot Mode	**Disabled** Enabled	**Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.**
Dark Boot	Disabled **Enabled**	**If enabled, system comes up with a blank screen instead of the diagnostic screen during bootup.**
‣ Boot Device Priority	**sub menu**	**Opens boot device priority sub menu**
Onboard LAN RPL ROM	Disabled **Enabled**	**Enables Remote Program Load ROM of the onboard LAN controller. Supportes Intel PXE. See www.support.intel.com/support/desktopmgmt/pxepdk.htm. for more information**

The Boot Device Priority Menu

This menu allows to select the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list. The items on this menu each may represent the first of a class of items. For example, if you have more than one hard disk drive, Hard Drive represents the first of such drives as specified in the Hard Drive menu described below.
To change the order select the device you want to change and press <-> to decrease or <+> to increase priority.

Feature	Option	Description
‣ Removable Devices	**boot priority & sub menu**	**Sets boot priority of Removable Devices as described in the respective sub menu.**
‣ Hard Drives	**boot priority & sub menu**	**Sets boot priority of Hard Disks as described in the respective sub menu.**

ATAPI CD-ROM Drive	boot priority	Sets boot priority of ATAPI CD:ROM Drives.
▸ Network Boot	boot priority & sub menu	Sets boot priority of Network Adapters as described in the respective sub menu.

The Removable Devices Menu

If you have more than one Removable Media drive, select Removable Devices and press <Enter> to display the Removable Media menu and choose which drive is represented in boot-order menu. Note: The standard 1.44MB floppy drive is referenced as „Legacy Floppy Drives".

The Hard Drive Priority Menu

If you have more than one bootable hard drive, select Hard Drive and press <Enter> to display the Fixed Disk Menu and choose the boot priority.

The Network Boot Priority Menu

If you have more than one bootable network adapter in the system, select Network Boot and press <Enter> to display the available network adapters and choose the boot priority.

The Boot First Menu

Display the Boot First Menu by pressing <Esc> during POST. In response, the BIOS first displays the message „Entering Boot Menu..." and then displays the Boot Menu at the end of POST.

Use the menu to select any of these options:

- **Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.**
- **Enter Setup**
- **Press <Esc> to continue with the existing boot sequence.**

9.3 BIOS Update with Phoenix Phlash

Phoenix Phlash gives you the ability to update your BIOS from a floppy disk without having to install a new ROM chip. Phoenix Phlash is a utility for „flashing" a BIOS to the Flash ROM installed on the *MOPS/520*.

Use Phoenix Phlash for the following tasks only:
- **Update the current BIOS with a newer version**
- **Restore a BIOS when it has become corrupted (see below)**

Phoenix Plash can be downloaded as a compressed file called CRISP489.ZIP from the JUMPtec® wep page and contains the following files:

MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette
CRISBOOT.BIN	The Crisis Recovery boot sector code
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode
PHLASH.EXE	Programs the flash ROM
WINCRISIS.EXE	Executable file for creating the Crisis Recovery Diskette from Windows
WINCRISIS.HLP	The help file of WINCRISES.EXE
PLATFORM.BIN	Performs platform-dependent functions
BIOS.ROM	Actual BIOS image to be programmed into flash ROM

To install Phoenix Phlash on your hard disk, unzip the content of CRISP489.ZIP into a local directory, presumable C:\PHLASH.

To create the Crisis Recovery Diskette insert a clean diskette into drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette:

MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode
PHLASH.EXE	Programs the flash ROM
PLATFORM.BIN	Performs platform-dependent functions

BIOS.ROM	Actual BIOS image to be programmed into flash ROM

If the BIOS image (BIOS.ROM) changes due to an update or bug fix, you can easily update the Crisis Recovery Disk. Simply copy the new BIOS.ROM image onto the diskette.

You can run Phoenix Phlash in one of two modes:

- **Command Line Mode**
- **Crisis Recovery Mode**

Use the Command Line mode to update or replace your current BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type PHLASH. Phoenix Phlash will automatically update the BIOS. Phlash may fail if your system is using memory managers, in which case the utility will display the following message:

Cannot flash when memory manager are present.

If you see this message after you execute Phlash, you must disable the memory manager on your system!

9.4 Boot Block Support

Updating the BIOS may create a possible hazard: power failures or fluctuations that occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this possible hazzard the *MOPS/520* is equiped with a boot block Flash ROM. The boot block region contains a fail-safe recovery routine. If the boot block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a special crisis diskette (see above).

Additionally the end user can insert an update key into the parallel port to force initiating the boot block recovery routine.

For further information on the update key and the crisis diskette check the JUMPtec® web page.

10. HARDWARE DESCRIPTION

10.1 Élan™SC520 Microcontroller Features

The *MOPS/520* Board operates with the Élan™SC520 Microcontroller. This is a Integrated 32-Bit Microcontroller which provides following features:

- **Synchronous DRAM (SDRAM) controller**
- **33 MHz, 32-bit PCI bus Revision 2.2-compliant**
- **100-MHz and 133-MHz operating frequencies**
- **PCI 3.3V/5V tolerance interface**
- **Low-voltage operation (core V CC = 2.5 V)**
- **5-V tolerant I/O (3.3-V output levels)**
- **16-Kbyte write-back cache**
- **Enhanced DMA controller includes double buffer chaining, extended address and transfer counts, and flexible channel routing**
- **Two 16550-compatible UARTs operate at baud rates up to 1.15 Mbit/s with optional DMA interface**
- **Programmable interval timer (PIT)**
- **Real-time clock (RTC) with battery backup capability and 114 bytes of RAM**
- **Watchdog timer guards against runaway software**
- **Native support for pSOS, QNX, RTXC, VxWorks, and Windows® CE operating systems**
- **Enhanced programmable interrupt controller (PIC) prioritizes 22 interrupt levels (up to 15 external sources) with flexible routing**

10.2 Interrupts

IRQ0	**System Timer**	
IRQ1	**Keyboard**	
IRQ2	**Cascade**	
IRQ3	**COM 2**	**note (1)**
IRQ4	**COM 1**	**note (1)**
IRQ5	**CAN-Bus**	**note (1)**
IRQ6	**Floppy**	
IRQ7	**LPT 1**	
IRQ8	**Clock/Calendar**	
IRQ9	**Available**	
IRQ10	**COM 3**	**note (1)**
IRQ11	**COM 4**	**note (1)**
IRQ12	**PS/2 Mouse**	**note (1)**
IRQ13	**Numeric-processor**	
IRQ14	**IDE Channel 1**	
IRQ15	**not available**	

Notes:

(1) if serial ports, PS/2 mouse or CAN controller are disabled via system bios, these interrupts are available for other devices.

10.3 DMA

DMA 1	**Available**
DMA 2	**Floppy**
DMA 3	**Available**
DMA 5	**Available**

10.4 Watchdog Extension

With the aid of a special Interrupt 15h function, the watchdog on a JUMPtec board can be controlled very easily.

The respective functions have the following calling conventions:

Watchdog init	**Int 15h**	**00h**
Input:	**AH = E0h** **AL = 00h** **BX = timeout in 0.2sec increments** **CX = delay in 0.2sec increments** **DX = watchdog action (0 = reset, 1 = NMI)**	
Output:	**None**	
Description:	**This funcion is a public JUMPtec INT15h extension used to init the watchdog on JUMPtec boards.**	

Watchdog trigger	**Int 15h**	**01h**
Input:	**AH = E0h** **AL = 01h**	
Output:	**None**	
Description:	**This funcion is a public JUMPtec INT15h extension used to trigger the watchdog on JUMPtec boards.**	

Detailed description of the watchdog function:

Programming:

The function *Init watchdog* must be called only once. The three parameters *delay time*, *timeout time* an *trigger event* must be set. After initialisation the watchdog will be active only after the delay time has expired. The watchdog must be reset during the *timeout time* with the *trigger watchdog function*. Otherwise a RESET or NMI will occur depending on *trigger event*.

The trigger- and the delay time can be set in steps of 0.2 sec.
The theoretical maximum values are:

- **timeout time 65535*0.2sec. = 13107s @ 3h 38min**
- **delay time 32767*0.2sec. = 6553s @ 1h 49min**

NOTE:
The limits above apply to the Int 15h interface. Due to internal limitations of the MOPS/520 watchdog, only the following delay/timeout values actually can be set:

0.5s, 1s, 2s, 4s, 8s, 16s, 32s

The interface will internally round other settings to the actually possible time values.

Init Watchdog (Int 15h, AH=E0h)

Called with AX E000h
BX timeout time
BX = 0 ⇨ watchdog off. BX_{max} = 0FFFFh
CX delay time
CX = 0 ⇨ no delay. CX_{max} = 07FFFh
DX trigger event
DX = 0 ⇨ RESET, DX = 1 ⇨ NMI

Returns no
Example

```
mov   ax,0E000h    ; Watchdog set
mov   bx,5         ; 5*0,2s = 1s Timeout
mov   cx,5         ; 5*0,2s = 1s Delay
mov   dx,0         ; after Timeout and Delay generate RESET
int   15h
```

10.5 CAN-Bus

The Can-Bus on the *MOPS/520* Boards is based on INTEL® 82527 controller.

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

A PC82C251 from PHILIPS acts as a interface to the physical bus. This is a CAN transceiver for 24 V systems.

11. THE JIDA STANDARD

The JIDA Standard
JIDA is the abbreviation for JUMP*tec*® **Intelligent Device Architecture.**
Every board with onboard BIOS extension shall support the following function calls, which supply information about the board. JIDA functions are called via Interrupt 15h with AH=EAh, AL=function number, DX=4648h (security word), CL=board number (starting with 1).

The interrupt will return with CL#0, if a board with the number specified in CL does not exist. CL will be equal to 0 if the board number exists. In this case, the content of DX is used to determine, if operation was successful. DX=6B6Fh indicates successful operation, any other value indicates an error.
To get information about the installed boards following the JIDA standard, the following procedure is recommended:
Call "Get Device ID" with CL=1. The name of the first device installed will be returned. If result was "Board exists" (CL=0), increment CL and call "Get Device ID" again. Repeat until result is "Board not present" (CL#0). You now know the names of all boards within your systen that follow the JIDA standard. More information about a specific board may then be obtained by calling the appropriate inquiry function with the board's number in CL.

WARNING: **Association between board and board number may change due to configuration changes. Do** not rely on any association between board and board number**. Instead, always use the procedure described in the preceding paragraph first, to determine the association between board and board number.**

The manual and sample code for the JIDA is available from our webpage at www.jumptec.de.

12. NETWORK OPERATION

12.1 Overview

The Ethernet interface on *MOPS/520* is realized with the DM9102A from DAVICOM.

The DM9102A is a fully integrated and cost-effective single chip Fast Ethernet NIC controller. It is designed with the low power and high performance process. It is a 3.3V device with 5V tolerance so it supports 3.3V and 5V signaling.

The DM9102A provides direct interface to the PCI or the CardBus. It supports bus master capability and fully complies with PCI 2.2. In media side, The DM9102A interfaces to the UTP3,4,5 in 10Base-T and UTP5 in 100Base-TX. It is fully compliance with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9102A to take the maximum advantage of its abilities. The DM9102A is also support IEEE 802.3x full-duplex flow control.

The DM9102A provides following features:

- **Integrated Fast Ethernet MAC, Physical Layer and transceiver in one chip**
- **Comply with PCI specification 2.2**
- **PCI bus master architecture**
- **EEPROM 93C46 interface supports node ID accesses configuration information**
- **Comply with IEEE 802.3u 100Base-TX and 802.3 10Base-T**
- **Comply with IEEE 802.3u auto-negotiation protocol for automatic link type selection**
- **Full Duplex/Half Duplex capability**
- **Support IEEE 802.3x Full Duplex Flow Control**
- **Digital clock recovery circuit using advanced digital algorithm to reduce jitter**
- **High performance 100Mbps clock generator and data recovery circuit**
- **Provides Loopback mode for easy system diagnostics**

12.2 Software and driver setup

Please refer to the corresponding readme and setup/install files.

12.3 Ethernet Technical Support

Many problems can be solved with the latest drivers for the DAVICOM DM9102A controller. JUMP*tec*® provides you with the latest *tested* drivers, which might be quite different from the newest ones. Therefore feel free to contact the DAVICOM page for driver updates.
For further technical support, contact either JUMP*tec*® or get support information and download software updates from DAVICOM World Wide Web server.

DAVICOM World Wide Web server

Home: http://www.davicom.com.tw/
Drivers: http://www.davicom.com.tw/download/download_driver.asp

Before contacting JUMP*tec*® for technical support, be prepared to provide as much of the following information as possible.

1) **Adapter type**
2) **Adapter configuration**
3) **- I/O Base, Memory Base, I/O or memory mode enabled, IRQ, and DMA channel**
   - Configured for media auto-detect or specific media type (which type).
   (Record this information from the driver's sign-on message if possible.)
4) **Computer System's Configuration**
   - BIOS (make and version)
   - System make and model
   - CPU (type and speed)
   - System RAM
5) **Software**
   – DM9102A driver and version
   - Your network operating system and version
   - Your system's OS make/version (MS-DOS, Novell's DOS, Win95, WFWG, etc.)
   - Version of all protocol support files
   - Frame types supported by you server
6) **Contents of your configuration files**
   - CONFIG.SYS
   - AUTOEXEC.BAT
   - PROTOCOL.INI
   - NET.CFG FILE
   - WINDOW'S SYSTEM.INI (if using Windows client)
   - AUTOEXEC.NCF file
   - or similar
7) **Any Error Message displayed.**

13. SPECIFICATIONS

13.1 Mechanical Specifications

PC/104 Bus connector: **2 pieces of 2*32 pin male and 2*20 pin male connector**

PC/104plus connector **4*30 pin 2mm connector**

REMEMBER: The PC/104plus connector is without connector shroud. It's not possible to use a PC/104plus board with connector shroud at top at MOPS/520. This is only a mechanical limitation and does not reduce the functionality of MOPS/520. Please order a module without connector shroud or place MOPS/520 at top at the stack.

Module-dimensions: **length * width 95 mm * 90 mm (3,7" * 3,5 ")**

13.2 Electrical Specifications

Supply voltage: **5V DC +/- 5%**

Supply voltage ripple: **100 mV peak to peak 0 - 20 MHz**

Supply current (maximal): **1,7 A (with 64MB SDRAM, 16MB CHIPdisk, CAN Bus and Ethernet)**

Supply current (typical, DOS-Prompt):
with 133 MHz , 64 MB SDRAM, 16MB CHIPdisk, CAN Bus and Ethernet **1,70A**

external RTC battery voltage **2,0..3,3V (typ. 2,5V)**
external RTC battery quiescent current **typ. 5uA**

The MOPS/520 is not a replacement for a backplane! It's strictly recommended to use all Power Pins on the PC/104 connector for power supply of the MOPS/520 and additional I/O cards.
The MOPS/520 is not a replacement for a backplane! It's not acceptabel to use only the power pins of the PC/104plus PCI connector for power supply of the full PC/104 stack.
The MOPS/520 is not a replacement for a backplane! Please refer the PC/104plus specification for the power supply of the MOPS/520 and all additional PC/104 I/O-cards.

13.3 Environmental Specifications

Temperature:	**operating**	**0 to +60 C ((*)with appropriate airflow))**
	non operating:	**-10 to +85 °C**
Humidity:	**operating:**	**10% to 90% (non-condensing)**
	non operating:	**5% to 95% (non-condensing)**

(*) The maximum operating temperature is the maximum measurable temperature on any spot on the modules´s surface. It is the user´s responsibility to maintain this temperature within the specification, which is set by the IC manufacturer.

14. PERIPHERAL INTERFACE

14.1 Keyboard, Reset, Battery, Speaker

PIN	Signal name	Function	5-pin diode keyboard adapter	6-pin minidin keyboard adapter (PS2)
1	SPKR	speaker output		
2	GND	ground		
3	RESIN	reset input 1		
4	/KLOCK	keyboard lock		
5	KDATA	keyboard data	2	1
6	KCLK	keyboard clock	1	5
7	GND	Ground	4	3
8	VCC	+5V	5	4
9	VBAT	VBAT input (max. 3,3V)		
10	POWERGOOD	reset input 2		

/KLOCK (keyboard lock)

input on CPU modules
output on any other module
input to the keyboard controller input port 1 bit 7 .

RESIN (reset input 1)

input on CPU modules
open collector output on all other module
When power good goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. This pin can also be used as a low active hardware reset for modules.

SPKR (speaker output)

open collector output on modules which can drive a loudspeaker.
input on modules which connect a 8 Ohm loudspeaker to this pin
An 8 Ohm loudspeaker is connected between SPEAKER and GND. Only one loudspeaker should be connected to this pin. Usually only the CPU drives this pin, however other modules can also use this signal to drive the system loudspeaker.

KDATA (keyboard data)

bi-directional I/O pin on CPU modules
Keyboard data signal.

KCLK (keyboard clock)

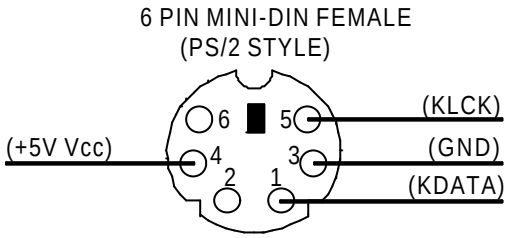
bi-directional I/O pin on CPU modules
Keyboard clock signal.

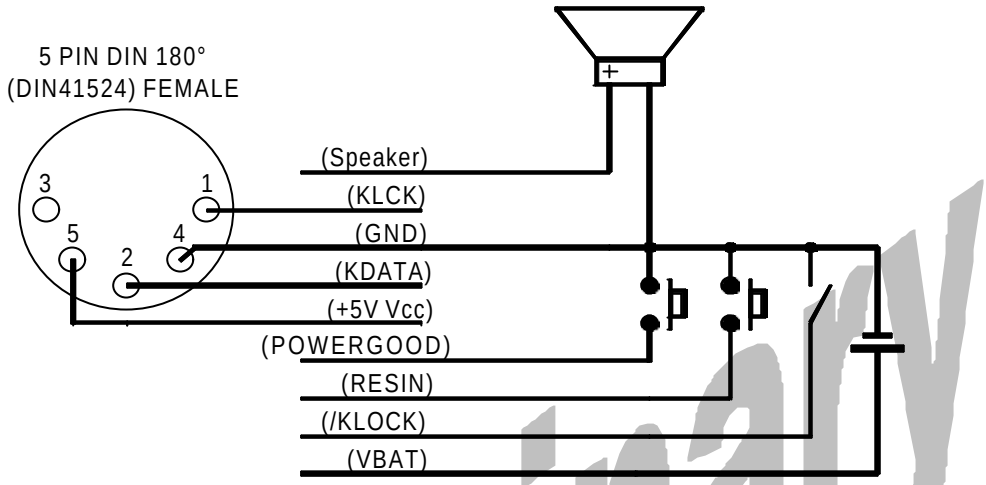
VBAT (system battery connection)

This pin connects a system battery to all modules.
The battery voltage has to be higher than 2.0V and lower than 3.3V. So a 3V battery is recommended.
Note, that there is no battery needed to hold the CMOS-setup data. Your configuration concerning hard disks, floppy drives etc. is automatically saved in an onboard FRAM. Nevertheless the battery is necessary to serve the CMOS date and time while power consumption is turned off.

POWERGOOD (reset input 2)

input on CPU modules
open collector output on all other module
When power good goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. This pin can also be used as a low active hardware reset for modules.



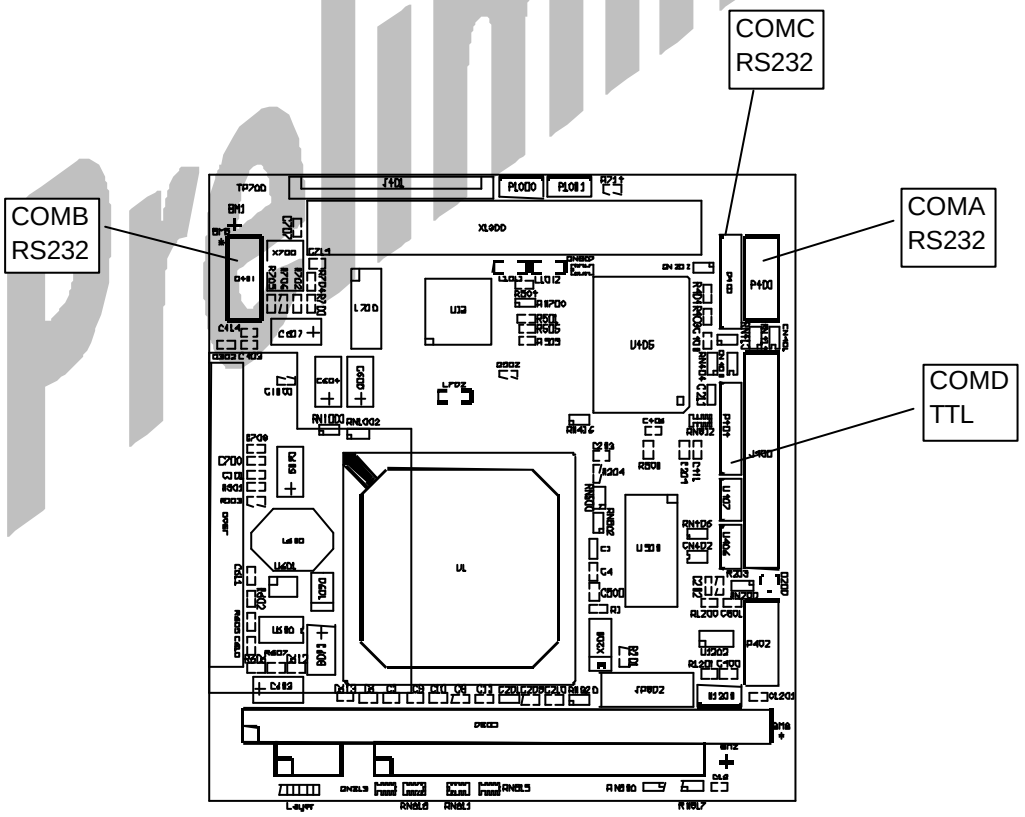


14.2 Serial Port COM 1, COM 2, COM 3 (RS232C) and COM 4 (TTL)

Pin	Signalname	In / Out	DSUB-25 (need Adapter)	DSUB-9 (need Adapter)
1	DCD	In	8	1
2	DSR	In	6	6
3	RxD	In	3	2
4	RTS	Out	4	7
5	TxD	Out	2	3
6	CTS	In	5	8
7	DTR	Out	20	4
8	RI	In	22	9
9	GND	--	7	5
10	+5V	--	--	--

For signal description please refer to additional literature.
The serial ports are completely compatible with the serial port implementation used on the IBM Serial Adapter.
COMA and COMB can be set to several I/O-addresses and IRQs in the setup. COMC and COMD are fixed mapped to the adresses and IRQs. See the table below for more informations.

Seriel Port	Possible I/O-adresses	Possible IRQs
COMA	3F8h, 2F8h, 3E8h, 2E8h	3, 4, 10
COMB	3F8h, 2F8h, 3E8h, 2E8h	3, 4, 11
COMC	3F8h	4
COMD	2F8	3



Please Note: Most OS detect the serial port with the I/O-adress 3F8h as COM1 an the port with the adress 2F8h as COM2. So if COMC and COMD are enabled they will detected as COM1 and COM2.

14.3 Parallel Port LPT 1

Pin	Signalname	Function	In / Out	DSUB-25 (need Adapter)
1	/Strobe		Out	1
3	Data 0		I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7		I/O	9
19	/ACK		in	10
21	BUSY		in	11
23	PAPER out		in	12
25	SEL out		in	13
2	/AUTOFD		out	14
4	/ERROR		in	15
6	/INIT		out	16
8	SEL in		out	17
26	Vcc	+ 5 V	--	NC
10,12	GND	Signal Ground	--	18 - 25
14,16	GND	Signal Ground	--	18 - 25
18,20	GND	Signal Ground	--	18 - 25
22,24	GND	Signal Ground	--	18 - 25

For signal description please refer to additional literature.
The Centronics printer interface can be programmed via the system setup menu.Refer to the periphal setup for more informations. The parallel port is completely compatible with the parallel port implementation used in the IBM PS-II-Parallel Adapter.

14.4 Floppy Connector

PIN	Signal	Function	Pin	Signal	Function
1	VCC	+ 5V	2	IDX	index
3	VCC	+ 5V	4	DS0	drive select 0
5	VCC	+ 5V	6	/DCHNG	disk change
7	NC	-	8	NC	-
9	NC	-	10	Mo0	motor on
11	NC	-	12	DIR	direction select
13	NC	-	14	STEP	step
15	GND	ground	16	WD	write data
17	GND	ground	18	WG	write gate
19	GND	ground	20	TR00	track 00
21	GND	ground	22	WP	write protect
23	GND	ground	24	RD	read data
25	GND	ground	26	SIDE	side one select

FOR SIGNAL DESCRIPTION PLEASE REFER TO ADDITIONAL LITERATURE.

14.5 IDE Connector for 2,5" Hard Disk

Pin	Signal	Pin	Signal
1	/RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	NC
21	NC	22	GND
23	/IOW	24	GND
25	/IOR	26	GND
27	NC	28	BALE
29	NC	30	GND
31	IRQ14	32	/IOCS16
33	SA1	34	NC
35	SA 0	36	SA2
37	/CS0	38	/CS1
39	/HDLED	40	GND
41	VCC	42	VCC
43	GND	44	NC

For signal description please refer additional literatur.

14.6 Ethernet Connector

Pin	Signalname	Function	In/Out
1	TXD+	100/10BASE-T Transmit	differential Output
2	TXD-	100/10BASE-T Transmit	differential Output
3	RXD+	100/10BASE-T Receive	differential Input
4	NC	Unused Pin	
5	NC	Unused Pin	
6	RXD-	100/10BASE-T Receive	differential Input
7	NC	Unused Pin	Output
8	NC	Unused Pin	Output

TXD+, TXD-

Differential output pair drives 10 and 100Mb/s Manchester encoded data to the 100/10BASE-T transmit lines.

RXD+, RXD-

Differential input pair receives 10 and 100Mb/s Manchester encoded data from the 100/10BASE-T receive lines.

14.7 USB1 and USB2 Connector

Pin	Pin function
1	+5V
2	USB-
3	USB+
4	GND

The power contacts on PIN 1 and 4 are are only usable for internal USB devices.
It's strictly recommended to use a fuse for power on external USB connectors.

14.8 Power Connector

Pin	Pin function
1	GND
2	+5V
3	VBAT
4	+12V
5	-5V
6	-12V
7	GND
8	+5V

Power Pins

The *MOPS/520* is a +5 V only module. Nevertheless the power connector offers the possibility to supply with the additional voltages +12V, -12V and -5V which may be needed by other boards in the PC/104 system. The power consumption of all available power pins on the *MOPS/520* is limited to 5A in total (1A per pin, with 2 pins on the power connector, 2 pins on the XT-bus and 1 pin on the AT-bus) and at GND up to 8A. Systems consuming more then 2A shouldn't be served over the power connector only. Systems consuming more then 5A must provide power supply through an additional connector on another board.

The MOPS/520 is not a replacement for a backplane! It's strictly recommended to use all Power Pins on the PC/104 connector for power supply of the MOPS/520 and additional I/O cards.

The MOPS/520 is not a replacement for a backplane! It's not acceptabel to use only the power pins of the PC/104plus PCI connector for power supply of the full PC/104 stack.

VBAT (system battery connection)

This pin connects a system battery to all modules.

The battery voltage has to be higher than 2.0V and lower than 3.3V. So a 3V battery is recommended.

Note, that there is no battery needed to hold the CMOS-setup data. Your configuration concerning hard disks, floppy drives etc. is automatically saved in an onboard FRAM. Nevertheless the battery is necessary to serve the CMOS date and time while power consumption is turned off.

14.9 CAN-Bus Connector

Pin	Pin function
1	CAN_L
2	CAN_H
3	VCC
4	GND

14.10 PC/104-Connector

Specification XT Bus

Pin	Signal Name	Pin	Signal Name
A1	/IOCHCK	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	/0WS
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND (*)
A11	AEN	B11	/SMEMW
A12	SA19	B12	/SMEMR
A13	SA18	B13	/IOW
A14	SA17	B14	/IOR
A15	SA16	B15	/DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	/DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	/REFRESH
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	/DACK2
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Specification AT Bus

Pin	Signal Name	Pin	Signal Name
C0	GND	D0	GND
C1	/SBHE	D1	/MEMCS16
C2	SA23	D2	/IOCS16
C3	SA22	D3	IRQ10
C4	SA21	D4	IRQ11
C5	SA20	D5	IRQ12
C6	SA19	D6	IRQ15 (**)
C7	SA18	D7	IRQ14
C8	SA17	D8	/DACK0 (**)
C9	/MEMR	D9	DRQ0 (**)
C10	/MEMW	D10	/DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	/DACK6 (**)
C13	SD10	D13	DRQ6 (**)
C14	SD11	D14	/DACK7 (**)
C15	SD12	D15	DRQ7 (**)
C16	SD13	D16	+5V
C17	SD14	D17	/MASTER (**)
C18	SD15	D18	GND
C19	GND (*)	D19	GND

(*) KEY PIN FOR PC/104; GND FOR PC/104+ - SPECIFICATION
(**) NOT SUPPORTET ON MOPS/520 BOARDS

For signal description and periphal driver current refer the PC/104 Specification.
Any signals are open collector for multiple sources and can not drive by TTL.

14.11 PC/104+ Connector

Pin	Signal name	Signal Name	Signal Name	Signal Name
	A	B	C	D
1	GND	Reserved	VCC	AD00
2	VCC	AD02	AD01	AD03
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VCC	AD10	GND
7	AD14	AD13	GND	AD12
8	VCC3*	C/BE1	AD15	VCC3*
9	SERR	GND	SB0	PAR
10	GND	PERR	VCC3*	SDONE
11	STOP	VCC3*	LOCK	GND
12	VCC3*	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	VCC3*
14	GND	AD16	VCC3*	C/BE2
15	AD18	VCC3*	AD17	GND
16	AD21	AD20	GND	AD19
17	VCC3*	AD23	AD22	VCC3*
18	IDSEL0 (AD20)	GND	IDSEL1 (AD21)	IDSEL2 (AD22)
19	AD24	C/BE3	VI/O	IDSEL3 (AD23)
20	GND	AD26	AD25	GND
21	AD29	VCC	AD28	AD27
22	VCC	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	VCC	GNT0
25	GNT1	VI/O	GNT2	GND
26	VCC	CLK0	GND	CLK1
27	CLK2	VCC	CLK3	GND
28	GND	INTD	VCC	RST
29	+12V	INTA	INTB	INTC
30	-12V	Reserved	Reserved	Reserved

*** NOT SUPPORTED ON MOPS/520**

For signal description and periphal driver current refer the PC/104+ Specification.

15. LITERATURE, STANDARDS, LINKS

It is not in the responsibility of JUMP*tec*® to supply you with informations about standard PC technology. Please find below a selection of different information sources for your convenience.

15.1 PC/104-Bus

- PC/104 Specification Version 2.3 **June 1996**
- PC/104-Plus Specification Version 1.1 **June 1997**
- PC/104 Consortium; **www.pc104.org**
- Embedded PCs, **Markt&Technik GmbH, ISBN 3-8272-5314-4 (german)**

15.2 ISA-Bus, Standard PS/2 - Connectors

- ISA System Architecture, **Addison-Wesley Publishing Company, ISBN 0-201-40996-8**
- AT BUS Design IEEE P996 Compatible, **Edward Solari, Annabooks San Diego CA. ISBN 0-929392-08-6 www.annabooks.com**
- PC Handbook, Sixth Edition, **John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1, www.annabooks.com**
- AT IBM Technical Reference Vol 1&2, **1985**
- ISA Bus Specifications and Application Notes, **January 30, 1990, Intel**
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, **Compaq 1989**
- Personal Computer Bus Standard P996, **Draft D2.00, January 18, 1990, IEEE Inc**
- Embedded PCs, **Markt&Technik GmbH, ISBN 3-8272-5314-4 (german)**
- **ePanorama PC Hardware Linkpage http://www.us-epanorama.net/pc/**

15.3 RS232C

- **EIA-232-E Interface between data terminal equipment and date circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)**

National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering „232“ as search criteria to get a current list of related application notes.

15.4 USB

The USB specification maybe obtained from the USB Implementers Forum web site at www.usb.org

15.5 PCI

The PCI specification maybe obtained from the PCI Special Interest Group web site at http://www.pcisig.com/.

16. DOCUMENT REVISION HISTORY

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