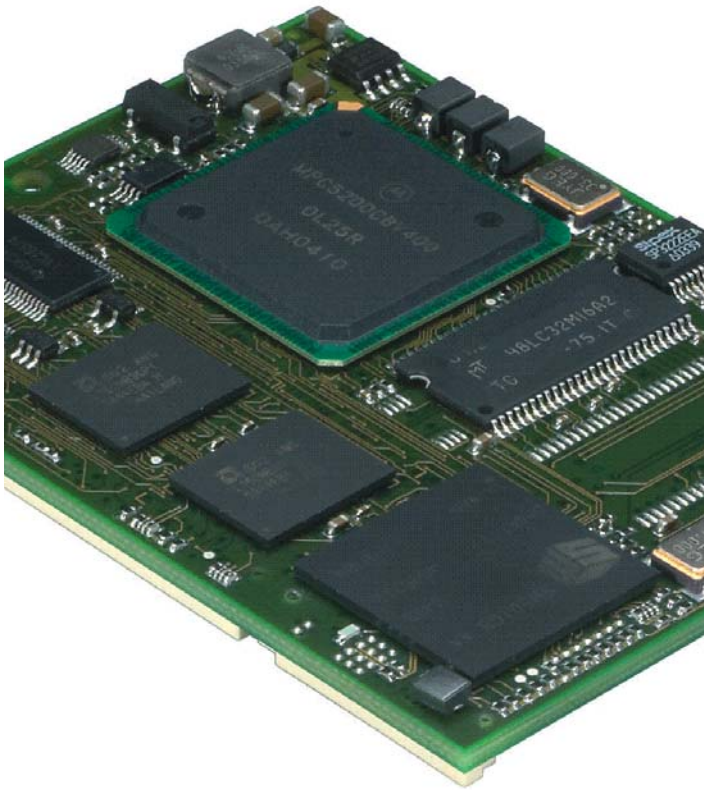
The key
to the embedded world



TQM5200
Hardware Manual
Rev.204

1 ABOUT THIS MANUAL

1.1 Table of Contents

1.2 Illustrations

1.3 Tables

1.4 Terms and Conventions

Symbol/Tag	Description
	This symbol represents the handling of electrostatic - sensitive modules and/or components. These components are often damaged/destroyed with the transmission of a voltage higher than about 50V. Human body usually notices electrostatic discharges only above approximately 3,000V.
	This symbol indicates the possible use of voltages greater than 24V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage/destruction of the component.
	This symbol indicates the possible source of danger. Acting against the procedure described can lead to possible damage to your health and/or cause damage/destruction of the material used.
	This symbol represents important details or aspects for working with TQ products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
`Instructions / Examples`	Examples of application. e.g. • Specifying memory partitions • Processing a script • .....
Reference	Cross-reference to another section, figure or table.

1.5 Acronyms and Definitions

The following terminology and abbreviations are used:

Acronym	Full Form
BDM	Background Debug Mode
CPU	Central Processing Unit
CAN	Controller Area Network
EEPROM	Electrically Erasable Programmable Read-Only Memory (Byte wise re-writable)
EMI / EMC	Electro Magnetic Interference / Electro Magnetic Compatibility
Flash	Electrically Erasable Programmable Read-Only Memory (Block Erase)
JTAG	Joint Test Action Group
MCU	Memory Control Unit
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface Mounted Device

1.6 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Handling/ESD Tips

General handling of your TQ products

The handling and use of your TQ product may be done exclusively by qualified personnel.

Ensure that while using your TQ product, particularly while plugging in/out of modules, changing jumper settings, or connecting other external devices, the power supply is not connected to your TQ product. Violation of this guideline can result in damage/destruction of the module and cause danger to your health.

Improper handling of your TQ product would render the guarantee invalid.

1.8 Proper ESD handling

The ESD components must be used in workplaces which are apt for the handling them in order to avoid damage or destruction.

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1.13 Revision History

Rev.	Date	Name	Pos.	Modification
049	08.08.04	VJU		Creation (Provisional Specification)
050	09.08.04	ANW		Adaptations
201	17.01.05	VJU		Finalizations
202	16.02.05	VJU		Revision after internal checks
203	25.02.05	VJU	4.2	Add dimensional drawing
	14.04.05	ANW		Revision
204	10.05.05	DEN		Translation

2 PRODUCT IDEA

While designing the TQM5200, particular importance has been given to the compact external dimension. With just 80x60 mm², the TQM5200 has a very compact form factor. Apart from requiring less space on the Basis Board, it also has advantages with mechanical pressure, e.g. shock or vibration. Robustness and industrial suitability were also important criteria according to which, the connector system of the module was selected. Based on the experience, one uses a 0.8mm Mezzanine- connector system.

3 FUNCTIONALITY AND SYSTEM ARCHITECTURE

The TQM5200 is a Mini module with MPC5200 PowerPC-CPU (Freescale) and SM501 Graphic-Controller by Silicon Motion.

3.1 System architecture / Block Circuit Diagram

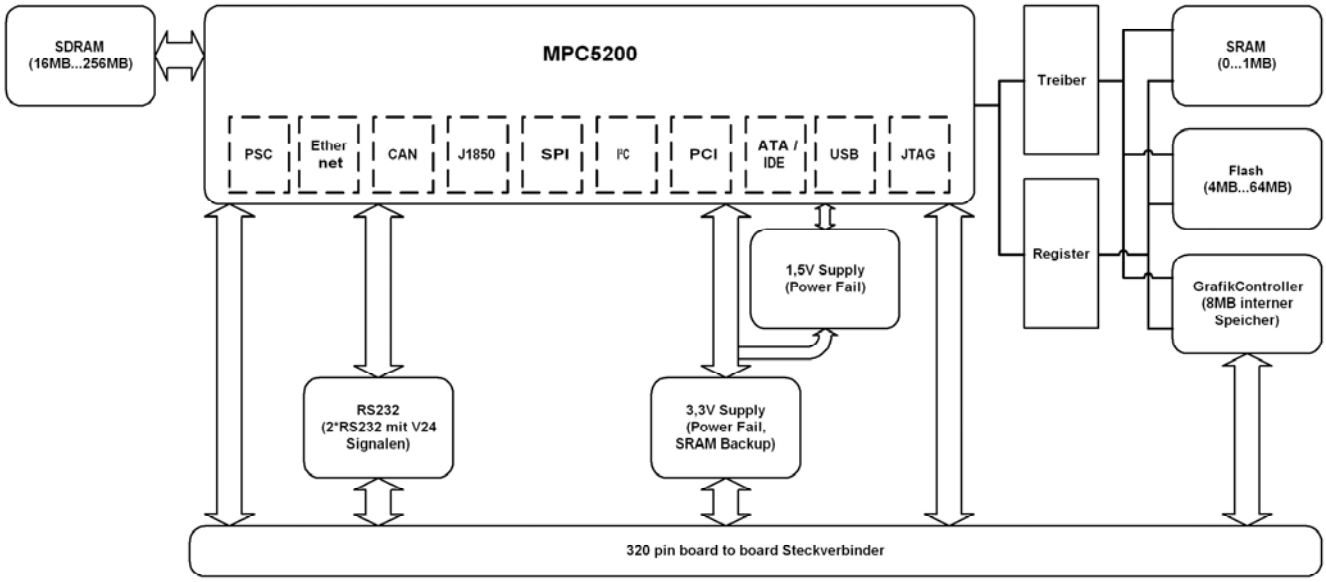


Illustration 1: Block Circuit Diagram TQM5200

3.2 Functionality (Brief description)

The TQM5200 includes the following system components:

- Freescale PowerPC Processor MPC5200 up to 400MHz with MPC603e Processor Core
- 33MHz Oscillator for the CPU-Clock
- Silicon Motion Graphic Controller SM501 with 8MB internal graphic memory
- 24MHz Oscillator for the Graphic Controller
- SDRAM: 16MB up to 128MB[1] / 256MB[2]; 32Bit data length
- Flash: 4MB up to 32MB Flash[3] Data length : 32Bit
- SRAM: 512kByte or 1Mbyte, data length: 16-Bit. Possibility of buffering the battery by the Basis-Hardware
- Serial EEPROM: 0kBit up to 64kBit, I^2C-Bus
- CPLD for Reset-Configuration and activation of SRAM and Graphic-Controller
- Driver for two serial interfaces (RxD, TxD)
- 32-Bit Bus driver and 24-Bit Address Register for module components at the Local-Plus-Bus
- COP/JTAG Interface
- Single Power Supply 3.3V
- Switch-Mode DC/DC Converter on the Module (3.3V on 1.5V)
- Linear DC/DC Converter on the Module (3.3V on1.8V)
- 1.5V Supervisor/Power-Fail-Logic
- 1.8V Supervisor/Power-Fail-Logic
- 3.3V Supervisor/Power-Fail-Logic with SDRAM Battery Backup
- 240 Pin + 80Pin (320Pin) Board-to-Board connector system

Except the interface for the synchronous DRAM and the XTAL- Pins, all the micro-processor pins are led through two 120 pole module connectors. Further, all the pins from the Graphic Controller belonging to the LCD and CRT Interface are led through two 40 pole module connector.

With the exception of RS232-Transceicers, the Transceiver for Ethernet, USB, CAN, etc... are not placed on the module. Driver components are realized in the Basis-Hardware.

[1] With a memory bank for the MPC5200 Rev 1.2 (Chip masks Revision A)
[2] With two memory banks starting with MPC5200 Chip masks Revision B (from Q3/2005)
[3] 64 and128MB addressed by the Bank-Select-Bits

4 ELECTRONIC-SPECIFICATION

The Module is supplied with 3.3VDC. The Processor-Core-Voltage (1.5V) and the Core-Voltage for the Graphic Controller (1.8V) are generated by the voltage regulator from the input voltage (3.3V) on the module. As a standard product, TQM5200 is specified for a temperature range of 0°C....+70°C and optionally also for the temperature range of –40°C....+85°C.

4.1 System components

4.1.1 CPU

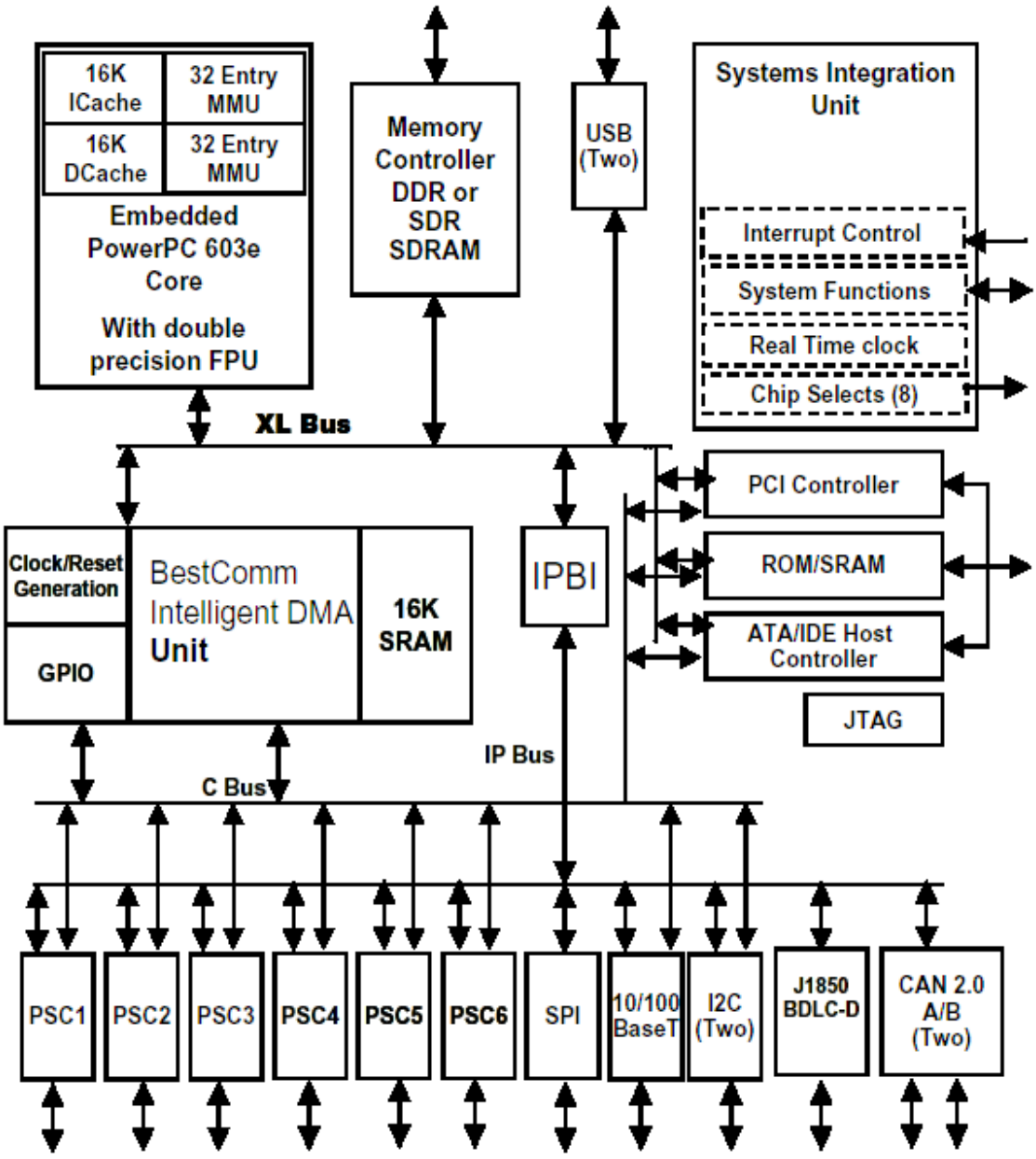


Illustration 2: Processor Block circuit diagram

CPU Main

- MPC603e series G2_LE core
- Superscalar architecture
- 760Mips at 400MHz (-40 to +85°C)
- 450Mips at 264MHz (-40 to +105°C)
- 16k Instruction cache, 16k Data cache
- Double precision FPU
- Instruction and Data MMU
- Standard & Critical interrupt capability

SDRAM / DDR Memory Interface

- up to 133MHz operation
- SDRAM and DDR SDRAM support
- 256-MByte addressing range per CS, Two CS available
- 32-bit data bus
- Built-in initialization and refresh

External Bus Interface

- Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
- 8 programmable Chip Selects
- Non multiplexed data access using 8/16/32 bit data bus with up to 26 bit address
- Short or Long Burst capable
- Multiplexed data access using 8/16/32 bit data bus with up to 25 bit address

Peripheral Component Interconnect (PCI) Controller

- Version 2.2 PCI compatibility
- PCI initiator and target operation
- 32-bit PCI Address/Data bus
- 33 and 66 MHz operation
- PCI arbitration function

ATA Controller

- Version 4 ATA compatible external interface

6 Programmable Serial Controllers (PSC)

- UART or RS232 interface
- CODEC interface for Soft Modem, Master/Slave CODEC Mode, I2S and AC97
- Full duplex SPI mode
- IrDA mode from 2400 bps to 4 Mbps

Fast Ethernet Controller (FEC)

- Supports 100Mbps IEEE 802.3 MII, 10Mbps IEEE 802.3 MII, 10Mbps 7-wire interface

Universal Serial Bus Controller (USB)

- Version 1.1 Host only
- Support for two independent USB slave ports

Two Inter-Integrated Circuit Interfaces (I2C)
- Serial Peripheral Interface (SPI)

Dual CAN 2.0 A/B Controller (MSCAN)
- Motorola Scalable Controller Area Network (MSCAN) architecture
- Implementation of version 2.0A/B CAN protocol
- Standard and extended data frames

J1850 Byte Data Link Controller (BDLC)
- J1850 Class B data communication network interface compatible and ISO compatible for low speed (<125kbps) serial data communications in automotive applications.
- Supports 4X mode, 41,6 kbps
- In-frame response (IFR) types 0, 1, 2, and 3 supported

! note !	**The functions described here are not available simultaneously. The PSC's functions are multiplexed. More information about it can be found in section 2 of the MPC5200 User-Manual.**

Table 1: CPU

Component	Manufacturer	Type	Temperature range
MPC5200CVB400	Freescale	400MHz PPC	-40°C - +85°C

4.1.2 CPU-Power-On Reset Configuration on the CPU-Pins

The Settings described in the table given below are accepted by HRESET# after the rising edge and by the CPU pins after the Hold-time of two clock cycles (SYS_XTAL) and are saved in the CDM Reset Configuration Register. The set configuration cannot be changed during the runtime of the CPU.

The Reset configuration is set through a CPLD. During the Reset phase, the configuration and the two clock cycles after the rising edge are set on the Config.-Pins of the CPU by the HRESET#. Then the CPLD-outlets are tristated. Wrong settings can lead to a system that cannot be booted!

The PLL configuration should be considered while setting. This configuration defines the XL-Bus frequency and the CPU-Core frequency. Settings for PCI and for the Local-Plus- Bus are derived from the XL-Bus-Frequency and can be changed during the runtime. Further, boot settings are done here, which are valid only for accessing the data via Boot-CS#. The accesses via CS0# to CS5# can be changed during the runtime.

Table 2: Reset Configuration

Reset Config Pin RST_CFGx	TQM5200 Startup Config.	CDM Reset Config. Register Bit PORCFG[x]	I/O Signal Name	Config Signal from CDM	Description
0	0	31	ATA_DACK#	ppc_pll_cfg_4	MPC5200 G2_LE PPC Core PLL Configuration
1	0	30	ATA_IOR#	ppc_pll_cfg_3	
2	0	29	ATA_IOW#	ppc_pll_cfg_2	
3	1	28	LP_RW	ppc_pll_cfg_1	
4	0	27	LP_ALE#	ppc_pll_cfg_0	
5	0	26	LP_TS#	xlb_clk_sel	bit=0: XLB_CLK=SYS_PLL FVCO/4 bit=1: XLB_CLK=SYS_PLL FVCO/8
6	0	25	USB1_1	sys_pll_cfg_0	bit=0: SYS_PLL FVCO=16x SYS_PLL_FREF bit=1: SYS_PLL FVCO=12x SYS_PLL_FREF
7	0	24	USB1_2	sys_pll_cfg1	bit=0: VCO = SYS_PLL_VCO bit=1: VCO = 2xSYS_PLL_FVCO
8	0	23	ETH0	boot_rom_mg	bit=0: No Boot in Most Graphics Mode bit=1: Boot in Most Graphics Mode
10	0	21	ETH2	ppc_msrip	Microprocessor Boot Address/Exception table location. bit=0: 0000_0100 (hex) bit=1: FFF0_0100 (hex)
11	1	20	ETH3	boot_rom_wait	Bit=0: 4 IP bus clocks of wait state1 bit=1: 48 IP bus clocks of wait state1
12	0	19	ETH4	boot_rom_swap	Bit=0: no byte lane swap, same endian ROM image bit=1: byte lane swap, different endian ROM image
13	1	18	ETH5	boot_rom_size	For non-muxed boot ROMs: bit=0: 8bit boot ROM data bus, 24bit max boot ROM address bus bit=1: 16bit boot ROM data bus,16bit

Reset Config Pin RST_CFGx	TQM5200 Startup Config.	CDM Reset Config. Register Bit PORCFG[x]	I/O Signal Name	Config Signal from CDM	Description
					boot ROM address bus For muxed boot ROMs:2,3 boot ROM address is max 25 significant bits during address tenure. bit=0: 16bit ROM data bus bit=1: 32bit ROM data bus
14	1	17	ETH6	boot_rom_type	bit=0: non-muxed boot ROM bus, single tenure transfer. bit=1: muxed boot ROM bus, with address and data tenures, ALE and TS active.
15	0	16	ETH1	large_.ash_sel	bit=0: No Boot in Large Flash Mode bit=1: Boot in Large Flash Mode

4.1.3 CPU-Pulse generation

Two oscillators and quartz are placed on a module.

- 33MHz Oscillator for the CPU
- 24MHz Oscillator for the SM501 Graphic-Controller
- 32768 KHz Quartz for the MPC5200's RTC. For operating this RTC, 3.3 V supply voltage must be provided on the module. In order to reduce the quiescent current consumption for a system, it is suggested to introduce an external RTC on the Basis Board. An external RTC can e.g. be attached through a I2C-Bus.

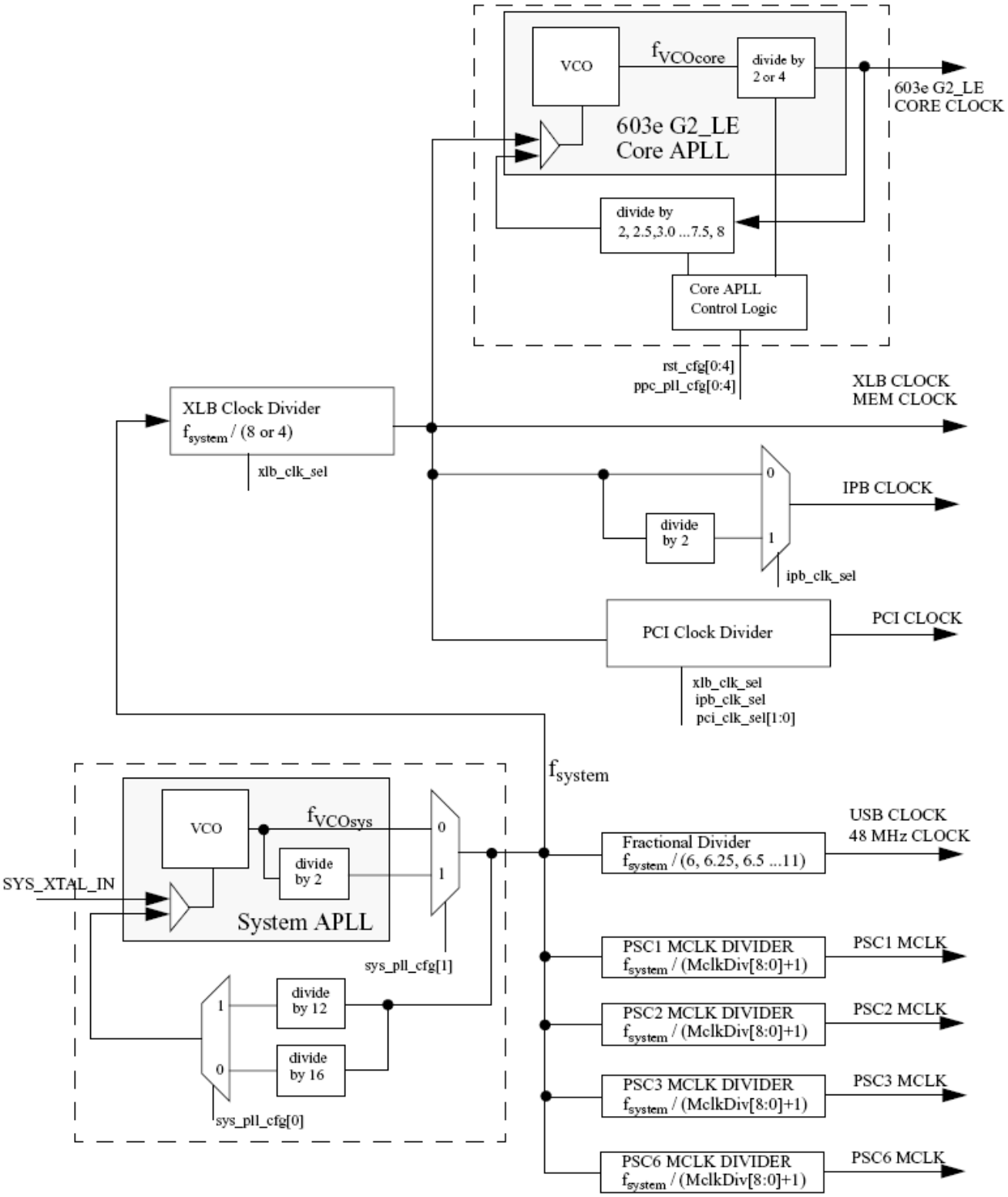
All the further clock frequencies used by the CPU are generated internally in the CPU from 33MHz.

Table 3: Oscillators and quartz for the MPC5200

Component	Manufacturer	Type	Temperature range
SX03-0507-E-50-W-33.000MHz	TJE	Oscillator 33 MHz	-40°C - +85°C
SX03-0507-E-50-W-24.000MHz	TJE	Oscillator 24 MHz	-40°C - +85°C
MC306	Epson / Seico	Quartz 32,768KHz	-40°C - +85°C

With the above described Reset Configuration-Register, the clock frequencies for the 33MHz initial pulses are set for the TQM5200 Module in such a manner that the following pulses are generated:

- XLB-Clk: 132 MHz
- IPB-Clk: 132 MHz
- PCI-Bus-Clk: 66 MHz
- Core-Clk: 396 MHz


VCO
$f_{VCOcore}$
divide by 2 or 4
603e G2_LE CORE CLOCK
603e G2_LE Core APLL
divide by 2, 2.5,3.0 ...7.5, 8
Core APLL Control Logic
rst_cfg[0:4]
ppc_pll_cfg[0:4]
XLB Clock Divider f_{system} / (8 or 4)
xlb_clk_sel
XLB CLOCK MEM CLOCK
divide by 2
0
1
IPB CLOCK
ipb_clk_sel
PCI Clock Divider
PCI CLOCK
xlb_clk_sel
ipb_clk_sel
pci_clk_sel[1:0]
f_{system}
VCO
f_{VCOsys}
divide by 2
SYS_XTAL_IN
System APLL
sys_pll_cfg[1]
divide by 12
divide by 16
sys_pll_cfg[0]
Fractional Divider f_{system} / (6, 6.25, 6.5 ...11)
USB CLOCK 48 MHz CLOCK
PSC1 MCLK DIVIDER f_{system} / (MclkDiv[8:0]+1)
PSC1 MCLK
PSC2 MCLK DIVIDER f_{system} / (MclkDiv[8:0]+1)
PSC2 MCLK
PSC3 MCLK DIVIDER f_{system} / (MclkDiv[8:0]+1)
PSC3 MCLK
PSC6 MCLK DIVIDER f_{system} / (MclkDiv[8:0]+1)
PSC6 MCLK

4.1.6 Flash memory

- 3,3 V Flash of the MirrorBit-Series (Spansion, AMD / Fujitsu), 16 Bit
- 1 Bank with two components and a Bus width of 32 Bit
- Connection to the multiplexed Local-Plus-Bus. The addresses are connected via a 25 Bit Address Register and the data is connected via a 32-Bit Bus driver.
- The ALE#-Signal is configured as “long“.
- Eight Wait states are used for accessing the Flash-Memory.
- Memory capacity 4 to 32 MB, with complete utilization of the Bank-Select-Bits 64/128MB
- Access time 120 ns
- As Chip Select, the Signal Boot-CS# (physical CS0#) is used so that one can boot from flash. The configuration for CS0 is described in table 9.

The Flash Status signal RY/BY# is not used, i.e. the course of the writing and deletion cycle must be maintained by Polling the Flash-Status bits (DQ7#, Toggle Bits etc.).

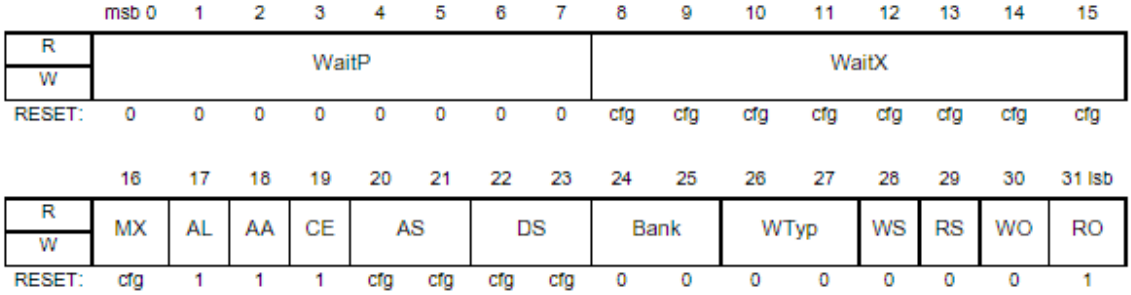


Illustration 4: Chip Select 0/Boot Configuration Register—MBAR + 0x0300

Table 6: Chip Select 0/Boot Configuration Register

Bits	Name	Setting	Description
0:7	WaitP	0x00	Number of wait states to insert. Can be applied as a prescale to WaitX or used by itself, as specified by WModel bits below. Wait states control how many PCI clocks the corresponding CS pin remains active.
8:15	WaitX	0x08	Base number of wait states to insert, or combined with WaitP as specified by WModel bits below. **cfg operation**—If rstcfg[11] (on pad_eth_03) is zero then 4 wait states are in effect, else 48 wait states are in effect. Wait States equals the number of PCI clocks from CS assertion to when data must be valid from boot device.
16	MX	1	MX bit specifies whether a transaction operates as multiplexed or non-multiplexed. A multiplexed transaction presents address and data in different tenures. During the address tenure, ALE is asserted. At the end of ALE, AD bus is switched to data tenure and CSx pin is asserted. 0=Non-multiplexed 1=Multiplexed **cfg operation**—If rstcfg[14] on pad_eth_06 is low, boot operation is non-multiplexed (single tenure), else boot operation is multiplexed (dual tenure).
17	AL	1	ALE length—multiplexed transactions only 0=ALE width is 1 internal IP bus clock 1=ALE width is 2 internal IP bus clocks At boot time, internal IP bus clock is twice the frequency of the PCI clock. Therefore, AL defaults to 1 (2 IP bus clocks) for boot device.

18	AA	0	ACK Active—multiplexed transactions only. This bit defines whether ALE input is active or not. If AA is 1, programmed wait states can be overridden when/if the external device drives the ACK input low. If AA is 0, the ACK input is ignored. Wait states are still in effect. If no ACK is received, cycle terminates at end of wait state period. **cfg operation**—If rstcfg[14] on pad_eth_06 is high, indicating multiplexed mode boot device, then AA is assumed high as well. This lets the boot device shorten the Wait State period by asserting the ACK input.
19	CE	1	An individual Enable bit—allows CS operation for the corresponding CS pin. CE must be high to allow operation. Register 6 master enable bit must also be high, except when CS[0] is used for boot ROM. 1 = Enable 0 = Disabled, register writes can occur but no external access is generated.
0:21	AS	11	Address Size field—defines size of peripheral Address bus (in bytes) and must be consistent with physical connections. 00 = 8 bits 01 = 16 bits 10 = 24 bits 11 = > 25 bits See documentation for Physical Connection requirements.The combination of address size, data size, and transaction Mode (MX) must be consistent with the peripheral physical connection. In case of a multiplexed transaction, the entire address is driven regardless of address size field. **cfg operation**—If rstcfg[13] on pad_eth_05 is low, then the address size for nonmultiplexed boot device is set to 24 bits (AS=10), else the boot device is treated as a 16 bit address (AS=01) device. For multiplexed mode boot devices the maximum 25 bits of address is always driven. This rstcfg bit more particularly affects the DS field below, and can be thought of as the “small” or “big” data size config bit.
22:23	DS	11	Data Size field—represents the peripheral data bus size (in bytes): 00=1Byte 01=2Bytes 10=3Bytes (**Not Supported**) 11=4Bytes **cfg operation**—If rstcfg[13] on pad_eth_05 is low, then the data size for non-multiplexed boot device is set to 8 bits (DS=00), else the boot device is treated as a 16 bit (DS=01) device. For multiplexed mode boot device the selection is 16 bit data or 32 bit data respectively.
24:25	Bank	00	Bank bits—are reflected on external AD lines (AD[26:25]) during Address tenure of a multiplexed transaction. Register bit 24 is the msb and appears on AD[26].
26:27	WModel	11	Wait state type bits—define the application of wait states contained in WaitP and WaitX fields, as follows: 00 = WaitX is applied to read and write cycles (WaitP is ignored). 01 = WaitX is applied to Read cycles, WaitP is applied to Write cycles. 10 = WaitX is applied to Reads, WaitP/WaitX (16-bit value) is applied to Writes. 11 = WaitP/Waitx (as a full 16-bit value) is applied to Reads and Writes.

28	WS	0	Write Swap bit—If high, Endian byte swapping occurs during writes to a peripheral. • For 8-bit peripherals, this bit has no effect. • For 16-bit peripherals, byte swapping can occur. • For 32-bit peripherals (possible in MUXed mode only) byte swap can occur. 1 = swap 0 = NO swap 2-byte swap is AB to BA, 4-byte swap is ABCD to DCBA. **NOTE:** Transactions at less than the defined port size (i.e.., data size) apply swap rules as above, according to the current transaction size.
29	RS	0	Read Swap bit—Same as WS, but swapping is done when reading data from a peripheral. 1 = swap 0 = NO swap **cfg operation**—If rstcfg[12] on pad_eth_04 is low, data from the boot device is Endian swapped when read. This only has effect for boot devices configured as 16- or 32-bit data size.
30	WO	0	Write Only bit—If bit is high, the peripheral is treated as a write-only device. An attempted read access results in a bus error (as dictated by Chip Select Control Register EBEE bit) and/or an interrupt (as dictated by Chip Select Control Register IE bit). In any case, no transaction is presented to the peripheral. A bus error means the internal cycle is terminated with a transfer error acknowledge (ips_xfr_err assertion to IP bus, TEA assertion to XL bus).
31	RO	0	Read Only bit—If bit is high, the peripheral is treated as a read-only device. An attempted write access results in a bus error (as specified by Chip Select Control Register EBEE bit) and/or an interrupt (as specified by Chip Select Control Register IE bit). In any case, no transaction is presented to the peripheral. **NOTE:** This bit is high from Reset, indicating Boot Device is Read-Only.

Table 7: Flash-Memory component

Component	Manufacturer	Model	Temperature range
Am29LV160MB90PCI	Spansion / AMD	Flash MirrorBit, 1 M * 16	-40°C - +85°C
Am29LV320MB120PCI	Spansion / AMD	Flash MirrorBit, 2 M * 16	-40°C - +85°C
Am29LV640MB120PCI	Spansion / AMD	Flash MirrorBit, 4 M * 16	-40°C - +85°C
Am29LV128ML123RPCI	Spansion / AMD	Flash MirrorBit, 8 M * 16	-40°C - +85°C
Am29LV256ML113RPGI	Spansion / AMD	Flash MirrorBit, 16 M * 16	-40°C - +85°C

With the exception of Am29LV256M, all the components have a 64-ball-Fortified-BGA-construction form with dimensions 13*11mm. Am29LV256M has a 64-ball-Fortified-BGA-construction form with dimensions 18*12mm. Am29LV256M is considered, while installing the component.

4.1.7 SRAM

- A memory bank with 16 Bit Bus width
- Memory capacity 512Kbyte or optional 1MByte
- Access time 70ns.
- Battery buffering of SRAM by the module connector (Standby-Power consumption, maximum 20µA)
- The SRAM is connected to the multiplexed Local-Bus-Plus of the processor through an Address Register and a bus driver.
- The ALE#-Signal is configured as long.
- Four wait states are used for accessing the SRAM.
- The CS2# -Signal is used for selection.

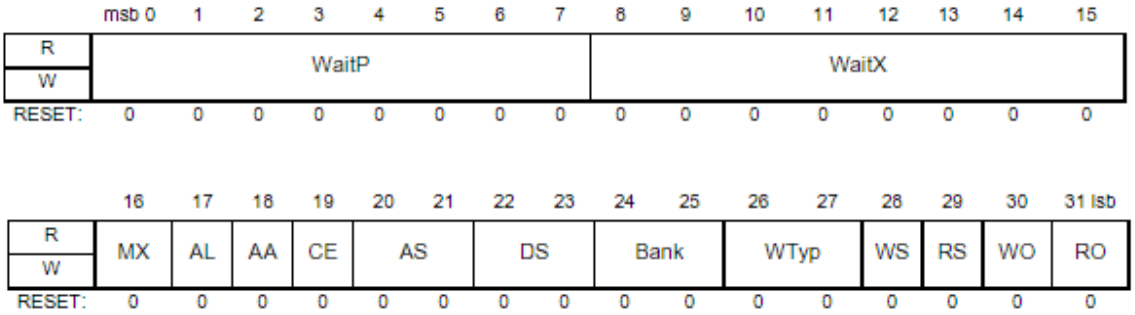


Illustration 5: Chip Select 2 Configuration Register—MBAR + 0x0308

Table 8: Chip Select 2 Configuration Register

Bits	Name	Einstellung	Description
0:7	WaitP	0x00	Number of Wait States
8:15	WaitX	0x04	The base number of wait states
16	MX	1	MX bit specifies whether transaction operates as multiplexed or non-multiplexed.
17	AL	1	ALE Length
18	AA	0	ACK Active
19	CE	1	Chip Enable bit
20:21	AS	11	Address Size field
22:23	DS	01	Data Size field
24:25	Bank	00	Bank bits
26:27	Wtyp	11	Wait state Type bits
28	WS	0	Write Swap bit
29	RS	0	Read Swap bit
30	WO	0	Write Only bit
31	RO	0	Read Only bit

Table 9: SRAM Memory module

Component	Hersteller	Typ	Temperaturbereich
K6X4016T3F-TF70	Samsung	SRAM 4-MBit	-40°C - +85°C
K6X8016T3B-TF70	Samsung	SRAM 8-MBit	-40°C - +85°C

4.1.8 EEPROM

The serial EEPROM can e.g. accept the characteristics of the module and customer specific parameter data. As against flash, individual memory cells can be deleted and overwritten in EEPROM. During delivery the EEPROM is empty. It can save e.g. the configuration data in a non-volatile manner.

- 0 - 64 KBit
- Activation via the I2C-Bus 2 of the CPU (I2C_2SCL / I2C_2SDA)
- Addresses of EEPROMs on 0b000

As against flash, individual memory cells can be deleted and overwritten in EEPROM. The EEPROM is not programmed during delivery.

Table 10: serial EEPROM

Component	Manufacturer	Model	Temperature range
M24C01WDW6	ST Micro- electronics	1-K EEPROM / TSSOP8	-40°C - +85°C
M24C02WDW6	ST Micro- electronics	2-K EEPROM / TSSOP8	-40°C - +85°C
M24C04WDW6	ST Micro- electronics	4-K EEPROM / TSSOP8	-40°C - +85°C
M24C08WDW6	ST Micro- electronics	8-K EEPROM / TSSOP8	-40°C - +85°C
M24C16WDW6	ST Micro- electronics	16-K EEPROM / TSSOP8	-40°C - +85°C
M24C32WDW6	ST Micro- electronics	32-K EEPROM / TSSOP8	-40°C - +85°C
M24C64WDW6	ST Micro- electronics	64-K EEPROM / TSSOP8	-40°C - +85°C

4.1.9 SDRAM

- Synchronous dynamic RAM, SDRAM, memory component 16 Bit
- Chip-Select through Mem_CS0 and Mem_CS1
- 132 MHz pulse
- 2 memory banks with 32 Bit width
- Memory structure for the normal temperature range: 16 Mbyte to 256Mbyte.
- Memory structure for the extended temperature range: 16 Mbyte to 128Mbyte.
- CAS Latency 3

While introducing the Micron 48LC16M16A2-75 SDRAMS while programming the mode-, control- and configuration register, following parameters must be considered:

Table 11: Parameter for SDRAM-Controller configuration

Description	Settings	Unit
Memory type	SDR	
XLB Speed	132	MHz
CAS (Read) Latency	3	Clock Cycles
THZ	5.4	ns
TDQSSmin	0	tCK
TWR	15	ns
TRCD	20	ns
TRFC	66	ns
TREF	64	ms
TREFI	7.8125	us
#ROWs	8192	
Mode Register Type	Normal	
Generate a Mode Register Set command	Yes	
Self Refresh Mode	No	
Automatic Refresh	Yes	
Extend Row and Column	Yes	
Precharge Control	A10	
Drive Rule for MDQ and MDQS	Drive except to read	
MDQS OE Mask	0	
Mode Register Locked	No	
Soft Refresh	No	
Soft Precharge All	No	

Following register settings are derived from the above-described parameters:

- Mode Register (MBAR+0x0100) => 0x008D0000
- Control Register (MBAR+0x0104) => 0xD14F0000
- Configuration Register 1 (MBAR+0x0108) => 0xD2322800
- Configuration Register 2 (MBAR+0x010C) => 0x8AD70000

The description of individual Register Bits can be found in section 8 SDRAM Memory Controller of theMP5200 User Manual [2].

The SDRAM components are listed in the following table.

Table 12: SDRAM components (Selection of all the released components)

Component	Manufacturer	Model	Temperature range
MT48LC32M16A2TG 75 (K4S511632M-TC75)[4]	Micron	SDRAM 32 M * 16	0°C – 70°C
MT48LC16M16A2TG 75 (K4S561632E-TI75)[1]	Micron	SDRAM 16 M * 16	-40°C - +85°C
MT48LC8M16A2TG 75 (K4S281632E-TI75)[1]	Micron	SDRAM 8 M * 16	-40°C - +85°C
MT48LC4M16A2TG 75 (K4S641632E-TI75)[1]	Micron	SDRAM 4 M * 16	-40°C - +85°C

[4] Alternative-model by Samsung

4.1.10 Graphic Controller

The SM501 by Silicon Motion is installed as the Graphic Controller.

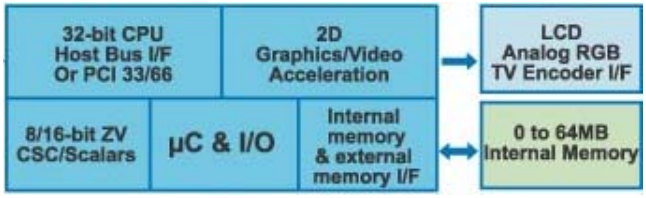


Illustration 6: SM501 Block Circuit Diagram

SM501 offers the following features:

Host Interface

- Direct 32-bit CPU and PCI interface
- Xscale (PXA-25x), IXP4XX, SH3/4, and MIPS direct CPU bus interface
- PCI v2.1 compliant

Display Support

- LCD (digital) and CRT (analog) with Dual Display
- LCD: 320x240 to 1024x768, 16/32-bit; 1280x1024 (16-bit only)
- CRT: VGA to SXGA, 16/32-bit
- Widescreen support up to 1280x768x16
- Hardware rotation
- Portrait and landscape display
- Can display different orientation on each output

2D/Video Acceleration Engine

- Optimized 128-bit 2D drawing engine
- Intelligent DMA command interpreter for enhanced performance
- Both front-end and back-end video engines
- 7 hardware display layers to support split screen, overlay, and alpha blending
- Per-pixel or planar alpha blend capability between layers
- Color space conversion from: YUV422 (YUY2 and UYVY),YUV420 (Planar4:1:1), YV12, IYUV (I420), IMC1, IMC2, IMC3, IMC4, NV12, NV21, RGB565, and RGBA888 to: RGB565 or RGBF888

Memory Configurations

- Dedicated graphics memory with 8MB

Package

- 19mmx19mm, 297 pin BGA (0.8mm ball pitch)
- Process: 0.18µ
- 0 & 8MB internal memory options

Table 13: Graphic-Controller

Component	Manufacturer	Model	Temperature range
SM501GE08	Silicon Motion	Graphic-Controller	-40°C - +85°C

The Graphic Controller is operated in the SH4 Mode with 66 MHz. For this, it is connected to the Local-Plus-Bus of MPC5200. The LP-Bus is selected in the memory of the CS1#-Signals through the Graphic Controller and is configured as a 32Bit Multiplex-Bus. The ALE# and the TS#-Signal are configured as long.

Access of SM501 is controlled by Acknowledge. Maximum number of Wait states are programmed for this type of accessing and for the addresses of CS1#-Signals. An access-cycle ends a pulse after the falling edge of the Acknowledge - Signals.

The values for the CS1# Configuration Register are listed in the following table.

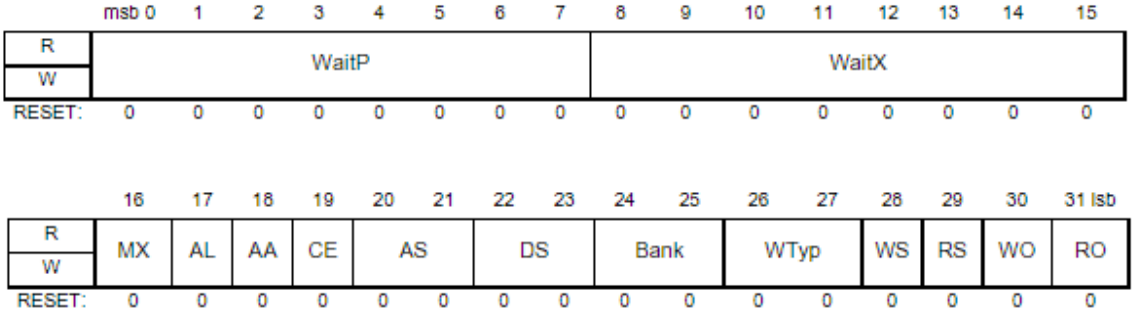


Illustration 7: Chip Select 1 Configuration Register—MBAR + 0x0304

Table 14: Chip Select 1 Configuration Register

Bits	Name	Setting*	Description
0:7	WaitP	0xff	Number of Wait States
8:15	WaitX	0xff	The base number of wait states
16	MX	1	MX bit specifies whether transaction operates as multiplexed or non-multiplexed.
17	AL	1	ALE Length
18	AA	1	ACK Active
19	CE	1	Chip Enable bit
20:21	AS	11	Address Size field
22:23	DS	11	Data Size field
24:25	Bank	11	Bank bits
26:27	Type	11	Wait state Type bits
28	WS	0	Write Swap bit
29	RS	0	Read Swap bit
30	WO	0	Write Only bit
31	RO	0	Read Only bit

* Description of the setting as in Chip Select 0 Table (Flash)

4.1.11 Pulse generation for the Graphic –Controller

A 24MHz Oscillator is installed for generating the pulse.

For applications with a TFT-Display on the Flat panel interface, a Low EMI Spread Spectrum Oscillator is optionally installed. This is an interface, where heavy demands are made on the electro-magnetic interfering radiation.

Table 15: Oscillators for the Graphic-Controller

Component	Manufacturer	Model	Temperature range
SX03-0507-E-50-W-24.000MHz	TJE	Oscillator 24 MHz	-40°C - +85°C

4.1.12 Diagnosis -LEDs

A red LED is provided as a status indicator for the CPU-Reset.

Table 16: Reset LED

Component	Manufacturer	Model	Temperature range
LGT679-C0	Osram	LED rot SO23	-40°C - +85°C

4.1.13 Serial interfaces

- The internal UART of MPC5200 by PSC1 or optionally the UART by PSC6 is connected to the module connector by a RS232-compatible Transceiver (RxD- / TxD-channel). It can be configured through resistance, which is used by both UARTs.
- The internal UART by PSC3 is connected to the module connector via the RS232-Transceiver (RxD- / TxD-Channel). Optionally, the UART by PSC3 can be separated from the RS232-Transceiver by removing the two Null-Ohm-resistance.
- max. 115200 Baud
- All operated signals are available on the module connector as inoperative also.

Table 17: RS232 Transceiver

Component	Manufacturer	Model	Temperature range
SP3222EEA	Sipex	Dual RS232 Transceiver	-40°C - +85°C

4.1.14 Module interfaces

With the exception of SDRAM-interface, the PLL supply and the XTAL-pins, all the other microprocessor pins are led through the connector. From the Graphic Controller, the CRT interface, the LCD interface as well as the GPIOs are connected to the connector. Moreover, there is a Master-Reset-Inlet, a SRAM-Backup-Power-Inlet as well as an operated RxD- und TxD-Signal of RS232-interfaces on a module connector.

The signals are allocated on the connector in such a manner that all processor signals, Non-CPU and PLD signals as well as the Reserve Pins are on two 120Pin-Connectors. The signals from the Graphic Controller are connected to two 40 pole power outlet box.

4.1.14.1 Connector

Board-to-Board-connection via a 120-pole and 40-pole connector with 0.8-mm spacing.

Board-to-Board Distance	Module				Base Board Connector		
	No. of Pin	**Qty**	**Supplier**	**Order No.**	**No. Of Pin**	**Supplier**	**Order No.**
5 mm	40	2	AMP	177983-1	40	AMP	177984-1
6 mm					40	AMP	179029-1
7 mm					40	AMP	179030-1
8 mm					40	AMP	179031-1
5 mm	120	2	AMP	177983-5	120	AMP	177984-5
6 mm					120	AMP	179029-5
7 mm					120	AMP	179030-5
8 mm					120	AMP	179031-5

The 0.8-mm-connector is available in different sizes. As an alternative, inter-mountable connectors by Fa. Berg are available.

Table 18: Module connector

Component	Manufacturer	Model
177983-1	AMP	Module connector 40 Pole
177983-5	AMP	Module connector 120 Pole

4.1.14.2 Pin Assignment

Table 19: Pin Assignment Connector X1 (Basis-Module-Connector 1)

Group	Function	MPC5200 BALL	Pin No. X1		MPC5200 BALL	Function	Group
Power	GND	-	2	1	-	3,3V	Power
Ethernet	ETH_16	L02	4	3	J04	ETH_17	Ethernet
	ETH_14	N04	6	5	N03	ETH_15	
	ETH_12	M02	8	7	M01	ETH_13	
Power	GND	-	10	9	L04	ETH_11	
Ethernet	ETH_10	J03	12	11	L01	ETH_9	
	ETH_8	M03	14	13	-	3,3V	Power
	ETH_6	N02	16	15	N01	ETH_7	Ethernet
Power	GND	-	18	17	L03	ETH_5	
Ethernet	ETH_4	J02	20	19	J01	ETH_3	
	ETH_2	K03	22	21	K02	ETH_1	
	ETH_0	K01	24	23	R01	IRQ3	Interrupt
Power	GND	-	26	25	-	3,3V	Power
Interrupt	IRQ2	P02	28	27	P01	IRQ1	Interrupt
	IRQ0	P03	30	29	V06	PCI_STOP#	PCI Control
PCI Control Control	PCI_TRDY#	W05	32	31	R02	PCI_RESET#	
Power	GND	-	34	33	Y07	PCI_PERR#	
PCI Control	PCI_SERR#	W08	36	35	Y06	PCI_IRDY#	
	PCI_REQ#	U01	38	37	-	3,3V	Power
	PCI_PAR	V07	40	39	R04	PCI_GNT#	PCI Control
Power	GND	-	42	41	W07	PCI_DEVSEL#	
PCI	PCI_ID_SEL	U02	44	43	Y02	PCI_CBE_3#	
	PCI_FRAME#	V05	46	45	W06	PCI_CBE_2#	
	PCI_CLOCK	T01	48	47	Y08	PCI_CBE_1#	
Power	GND	-	50	49	-	3,3V	Power
PCI / ATA / LP AD-Bus	EXT_AD_30	R03	52	51	W10	PCI_CBE_0#	PCI Control
	EXT_AD_28	T03	54	53	V01	EXT_AD_31	PCI / ATA / LP AD-Bus
	EXT_AD_26	T02	56	55	W01	EXT_AD_29	
Power	GND	-	58	57	Y01	EXT_AD_27	
PCI / ATA / LP AD-Bus	EXT_AD_24	U03	60	59	W02	EXT_AD_25	
	EXT_AD_22	V03	62	61	-	3,3V	Power
	EXT_AD_20	V02	64	63	W03	EXT_AD_23	PCI / ATA / LP AD-Bus
Power	GND	-	66	65	Y03	EXT_AD_21	
PCI / ATA / LP AD-Bus	EXT_AD_18	V04	68	67	Y04	EXT_AD_19	
	EXT_AD_16	W04	70	69	Y05	EXT_AD_17	
	EXT_AD_14	W09	72	71	U08	EXT_AD_15	
Power	GND	-	74	73	-	3,3V	Power
PCI / ATA / LP AD-Bus	EXT_AD_12	Y09	76	75	V08	EXT_AD_13	PCI / ATA / LP AD-Bus
	EXT_AD_10	Y10	78	77	V09	EXT_AD_11	
	EXT_AD_8	W11	80	79	V10	EXT_AD_9	
Power	GND	-	82	81	Y11	EXT_AD_7	
PCI / ATA / LP AD-Bus	EXT_AD_6	U11	84	83	W12	EXT_AD_5	
	EXT_AD_4	V11	86	85	-	3,3V	Power
	EXT_AD_2	V12	88	87	Y23	EXT_AD_3	PCI / ATA / LP AD-Bus
Power	GND	-	90	89	W13	EXT_AD_1	
PCI / ATA / LP AD-Bus	EXT_AD_0	V13	92	91	W16	LP_RW	LP Control
LP Control	LP_TS#	Y13	94	93	V14	LP_ALE#	
ATA ControControtro	LP_OE#	D08	96	95	U14	LP_ACK#	
Power	GND	-	98	97	-	3,3V	Power
ATA Control	ATA_IOR#	Y17	100	99	Y16	ATA_ISOLATION	ATA Control
	ATA_INTRQ	Y19	102	101	W17	ATA_IOW#	
	ATA_DACK#	Y18	104	103	W18	ATA_IOCHRDY	
Power	GND	-	106	105	V17	ATA_DRQ	
CS#	LP_CS5#	V16	108	107	non CPU	ATA_Reset#	

	LP_CS4#	Y15	110	109	-	3,3V	Power
	LP_CS2#	V15	112	111	W15	LP_CS3#	CS#
Power	GND	-	114	113	Y14	LP_CS1#	
CS#	LP_CS0#	W14	116	115	-	*Reserve 19*	Reserve
Reserve	*Reserve 20*	-	118	117	Non CPU	Start_L_H	Boot Ctrl
Power	GND	-	120	119	-	3,3V	Power

Table 20: Pin Assignment Connector X3 (Basis-Module-Connector 2)

Group	Function	MPC5200 BALL	Pin No. X3		MPC5200 BALL	Function	Group
Power	GND	-	2	1	-	3,3V	Power
Reset	RESIN#	non CPU	4	3	B13	HRESET#	Reset
	SRESET#	A14	6	5	A13	PO_RESET#	
CPU JTAG	CPU_JTAG_TDO	A02	8	7	A04	CPU_JTAG_TMS	CPU JTAG
Power	GND	-	10	9	A03	CPU_JTAG_TDI	
CPU JTAG	TEST_SEL_1	C03	12	11	B03	JCPU_JTAG_TRST#	
	CPU_JTAG_TCK	B04	14	13	-	3,3V	Power
	TEST_SEL_0	B01	16	15	A01	Test_Mode1	CPU JTAG
Power	GND	-	18	17	B02	Test_Mode0	
USB1	USB1_0	H01	20	19	H02	USB1_1	USB1
	USB1_2	H03	22	21	G01	USB1_3	
	USB1_4	G02	24	23	G03	USB1_5	
Power	GND	-	26	25	-	3,3V	Power
USB1	USB1_6	G04	28	27	F01	USB1_7	USB1
	USB1_8	F02	30	29	F03	USB1_9	
Timer	TIMER_0	Y20	32	31	V18	TIMER_1	Timer
Power	GND	-	34	33	D02	TIMER_3	
Timer	TIMER_2	D03	36	35	E03	TIMER_5	
	TIMER_4	D01	38	37	-	3,3V	Power
	TIMER_6	E02	40	39	E01	TIMER_7	Timer
Power	GND	-	42	41	C04	PSC3_9	PSC 3
PSC 3	PSC3_8	A05	44	43	B05	PSC3_7	
	PSC3_6	C05	46	45	A06	PSC3_5	
	PSC3_4	B06	48	47	C06	PSC3_3	
Power	GND	-	50	49	-	3,3V	Power
PSC 3	PSC3_2	A07	52	51	B07	PSC3_1	PSC 3
PSC 2	PSC2_4	A08	54	53	C07	PSC3_0	
	PSC2_2	A09	56	55	B08	PSC2_3	PSC 2
Power	GND	-	58	57	B09	PSC2_1	
PSC 2	PSC2_0	C09	60	59	B10	PSC1_3	PSC1
PSC 1	PSC1_4	A10	62	61	-	3,3V	Power
	PSC1_2	C10	64	63	A11	PSC1_1	PSC1
Power	GND	-	66	65	B11	PSC1_0	
PSC 6	PSC6_2	A12	68	67	C13	PSC6_3	PSC 6
	PSC6_0	B12	70	69	C11	PSC6_1	
RS232	RS232 TxD_1	non CPU	72	71	non CPU	RS232 RxD_1	RS232
Power	GND	-	74	73	-	3,3V	Power
RS232	RS232 TxD_2	non CPU	76	75	non CPU	RS232 RxD_2	RS232
I2C	SCL_2	V20	78	77	W20	SDA_2	I2C
	SCL_1	V19	80	79	W19	SDA_1	
Power	GND	-	82	81	non CPU	WP#/ACC	Flash Reset
GPIO	GPIO_WKUP_7	C12	84	83	non CPU	HRESETF#	
Battery	Vbatt 3V3	non CPU	86	85	-	3,3V	Power
LP_ByteSelect	SEL_B0#	non CPU	88	87	non CPU	SEL_B1	LP_ByteSelect
Power	GND	-	90	89	non CPU	SEL_B2	
LP_ByteSelect	SEL_B3#	non CPU	92	91	-	*Reserve 1*	Reserve
Reserve	*Reserve 2*	-	94	93	-	*Reserve 3*	
	Reserve 4	-	96	95	-	*Reserve 5*	
Power	GND	-	98	97	-	3,3V	Power
Reserve	*Reserve 6*	-	100	99	-	*Reserve 7*	Reserve
	Reserve 8	-	102	101	-	*Reserve 9*	
	Reserve 10	-	104	103	-	*Reserve 11*	
Power	GND	-	106	105	-	*Reserve 12*	

Reserve	*Reserve 14*	-	108	107	-	*Reserve 13*	
	Reserve 16	-	110	109	-	3,3V	Power
	Reserve 18	-	112	111	-	*Reserve 15*	Reserve
Power	GND	-	114	113	-	*Reserve 17*	
PLD-JTAG	JTAG_TDO	non CPU	116	115	non CPU	JTAG_TDI	PLD-JTAG
	JTAG_TCK	non CPU	118	117	non CPU	JTAG_TMS	
Power	GND	-	120	119	-	3,3V	Power

- 32 Connections GND
- 22 Connections 3,3V
- 20 Connections Reserve

Table 21: Pin Assignment Connector X2 (Graphic- Board-to-Board-Connector -Connector 1)

Group	Function	SM501 BALL	Pin No. X2		SM501 BALL	Function	
Power	GND	-	2	1	-	3,3V	Power
CLK_OF	SM501_CLKOF		4	3	AA14	SM501_USB-	USB
Power	GND	-	6	5	AA15	SM501_USB+	
GPIO	GPIO25	M20	8	7	M19	GPIO24	GPIO
	GPIO27	N18	10	9	M21	GPIO26	
	GPIO46	V19	12	11	N19	GPIO28	
Power	GND	-	14	13	-	3,3V	Power
GPIO	GPIO48	V21	16	15	V20	GPIO47	GPIO
	GPIO50	W17	18	17	W16	GPIO49	
LCD Interface	GPIO63	Z21	20	19	W18	GPIO51	
Power	GND	-	22	21	Z20	GPIO62	LCD Interface
LCD Interface	FP_CLK	AA10	24	23	W12	VDEN	
	FP_EN	V11	26	25	-	3,3V	Power
	FP_DISP	Y12	28	27	V123	BIAS	LCD Interface
Power	GND	-	30	29	Y11	FP_HSYNC	
CRT Interface	BLUE	AA12	32	31	W11	FP_VSYNC	
	GREEN	AA13	34	33	W13	HSYNC	CRT Interface
	RED	Y13	36	35	W14	VSYNC	
Power	GND	-	38	37	-	3,3V	Power
	GND	-	40	39	-	3,3V	

Table 22: Pin Assignment Connector X4 (Graphic- Board-to-Board-Connector -Connector 2)

Group	Function	SM501 BALL	Pin No. X4		SM501 BALL	Function	Group
Power	GND	-	2	1	-	3,3V	Power
LCD Interface	FP_22	Y10	4	3	W10	FP_23	LCD Interface
Power	GND	-	6	5	V9	FP_21	
LCD Interface	FP20	W9	8	7	Y9	FP_19	
	FP18	AA9	10	9	Z19	FP_17	
	FP_16	Y21	12	11	W8	FP_15	
Power	GND	-	14	13	-	3,3V	Power
LCD Interface	FP_14	Y8	16	15	AA8	FP_13	LCD Interface
	FP_12	V7	18	17	W7	FP_11	
	FP_10	Y7	20	19	Y20	FP_09	
Power	GND	-	22	21	AA7	FP_07	
LCD Interface	FP_8	Y19	24	23	Y6	FP_05	
	FP_6	W6	26	25	-	3,3V	Power
	FP_4	AA6	28	27	V5	FP_03	LCD Interface
Power	GND	-	30	29	Y18	FP_01	
LCD Interface	FP_2	W5	32	31	Y16	GPIO55	
	FP_0	Y17	34	33	N20	GPIO29	
	GPIO30	Z21	36	35	P19	GPIO31	
Power	GND	-	38	37	-	3,3V	Power
	GND	-	40	39	-	3,3V	

4.1.15 Service - Interfaces

4.1.15.1 Download-Interface

The serial interfaces on PSC1 acts as a Standard Download-interface (only RxD and TxD). For this purpose the serial interface on PSC1 is defined in the software (Universal-Boot) as the standard insulator pin.

As an alternative to PSC1-UART, the internal UART by PSC6 can be configured as the standard interface with the help of Zero-Ohm-Resistance. For this a modified Universal-Boot is required, which supports this interface as a standard.

4.1.15.2 COP/JTAG-Interface

All the connection of Freescale COP/JTAG interfaces (Debugging Interface) are available on the outer side. The COP/JTAG-Interface is finally installed on the basis circuit board through the connector. It has the following signals:

Table 23: COP/JTAG-Interface

Pin[5]	Signal name	Mode	Function
1	TDO	O	Test Data Output
3	TDI	I/O	Test Data Input
12, 16	GND	-	Ground
5	NC	-	NC
7	TCK	O	Test Clock
9	TMS	I/O	Test Mode Select
11	SRESET#	I	Soft Reset
13	HRESET#		Hard Reset
15	CKSTP_OUT#		Check Stop Out *(Protective circuit in the Basis HW)*
4	TRST#		Test Reset
6	3,3 V	O	Power

[5] Pin Assignment on the Starter kit (STK52xx) / the Module-Pins are listed in the table 22 connector X3

4.1.16 Supply

The supply voltage of the module is specified as follows:

- Module supply: 3.3 V ± 5 %
- Battery supply: 3.0 V .. 2.7V e.g. lithium battery CR2032

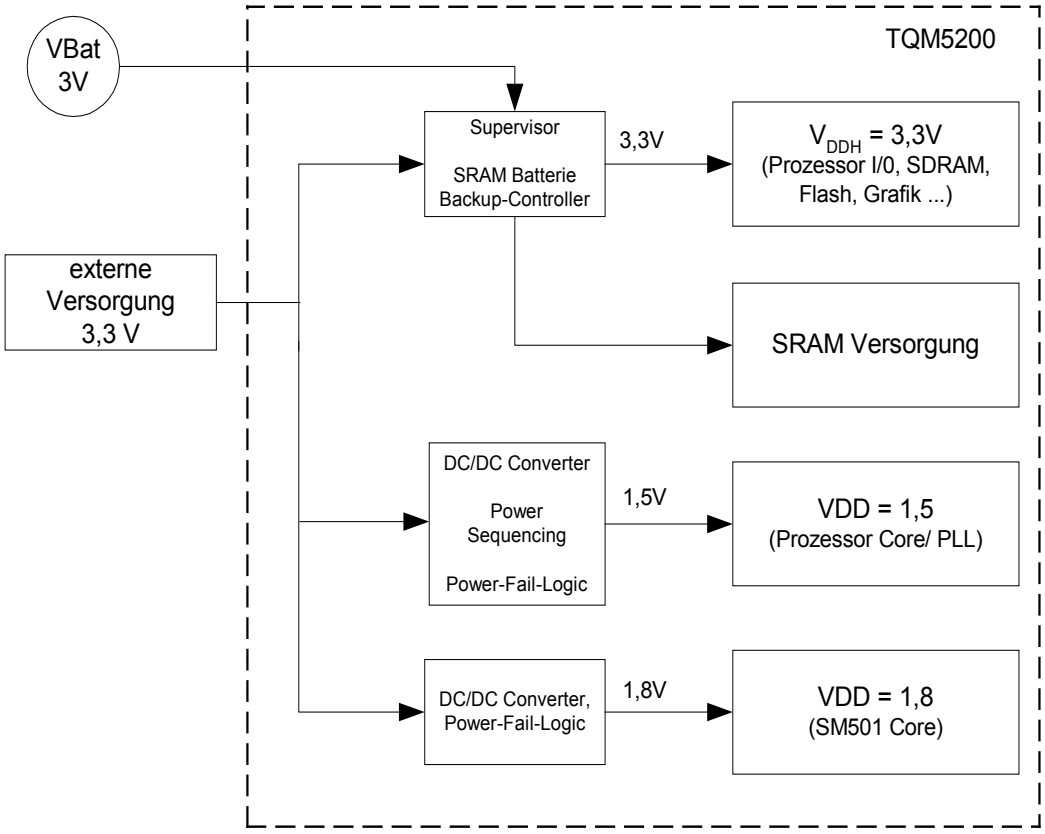


Illustration 8: Supply voltage

4.1.16.1 Tolerance of the external supply voltage

Tolerance of 3.3V supply

V_{CC3V3} = 3.3 V +/-5 % = 3.465 V .. 3.135 V

Reset-resolution from 3.06V

4.1.16.2 Internal voltage

MPC5200 Core-voltage 1.5V ± 5%
MPC501 Core-voltage 1.8V ± 5%

Table 24: DC/DC-Converter

Component	Manufacturer	Model	Temperature range
TPS4003DGQ	TI	Step-Down DC/DC Converter	-40°C - +85°C
LT1763CS8-1.8	LT	Voltage Regulator LDO	-40°C - +85°C

4.1.16.3 Maximum value for power consumption

	3.3V	**1.5V**	**1.8V**
Processor Core	-	800mA	-
Processor I/O	10mA[6]	-	-
Processor PLL	-	1,5mA	-
SDRAM	660 mA[7] / 1320mA[8]	-	-
SRAM	40 mA	-	-
Serial EEPROM	1 mA	-	-
Graphic Controller	160 mA	-	80mA
Flash	120 mA	-	-
Supervisor 3,3V	40 µA	-	-
Power-Fail-Logic 1,5V	10 µA	-	-
Power-Fail-Logic 1,8V	10 µA	-	-
RS232 Transceiver	1 mA	-	-
Bus driver	20mA	-	-
Address register	20mA	-	-
PLD	12mA	-	-
Amount	approx. 1110mA /1770 mA	approx. 800 mA	approx. 80mA
Amount to be fed in	**max. 1550mA[7] / 2200mA[8]**		

- [6] without external protective circuit
- [7] equipped SDRAM-Bank
- [8] Two equipped SDRAM-Banks

4.1.16.4 Typical values for power consumption

Following values are to be considered for the typical power consumption by TQM5200 without an external protective circuit:

- TQM5200 with Graphic-Controller (by connecting a Display) and an equipped SDRAM-Bank (128MB): approx **1100mA**
- TQM5200 without Graphic-Controller with 16 MB SDRAM: approx. **900mA**

4.1.16.5 Reset-Logic / Supervisor

The Reset-Logic has the following functions:

- Monitoring the voltage used on the module (3.3V, 1.8V, 1.5V)
- External Reset-Input
- Battery back up function for SRAM (Battery supply not on the module)
- Chip-Select-Gating for SRAM
- Reset-Status-Display through a red LED

4.2 Dimensions and structure

- The circuit board dimensions are 80 mm x 60 mm
- Size: Approx. 10 mm
- Free size under the module: Approx 2.9 mm

The illustration shows the TQM5200.

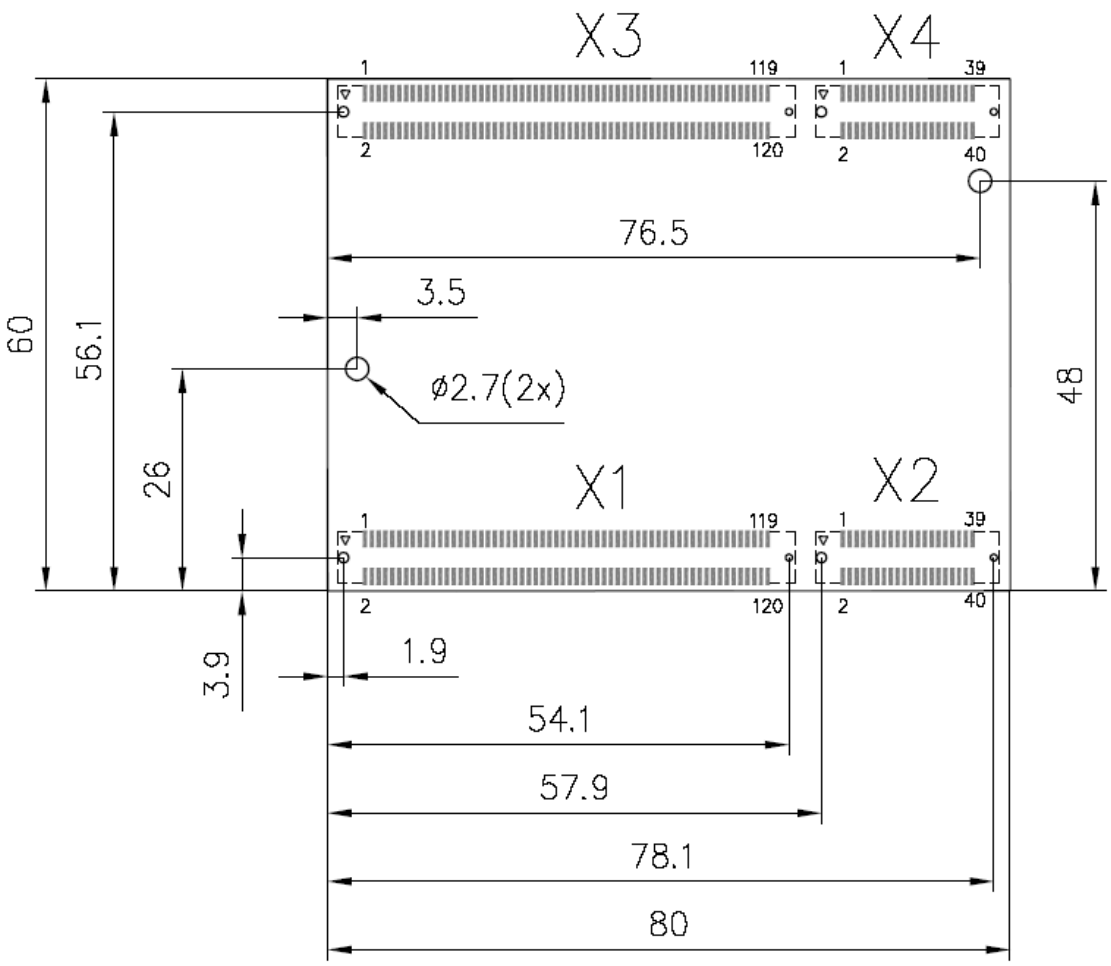


Illustration 9: Dimensional diagram. Top view through the conductor board

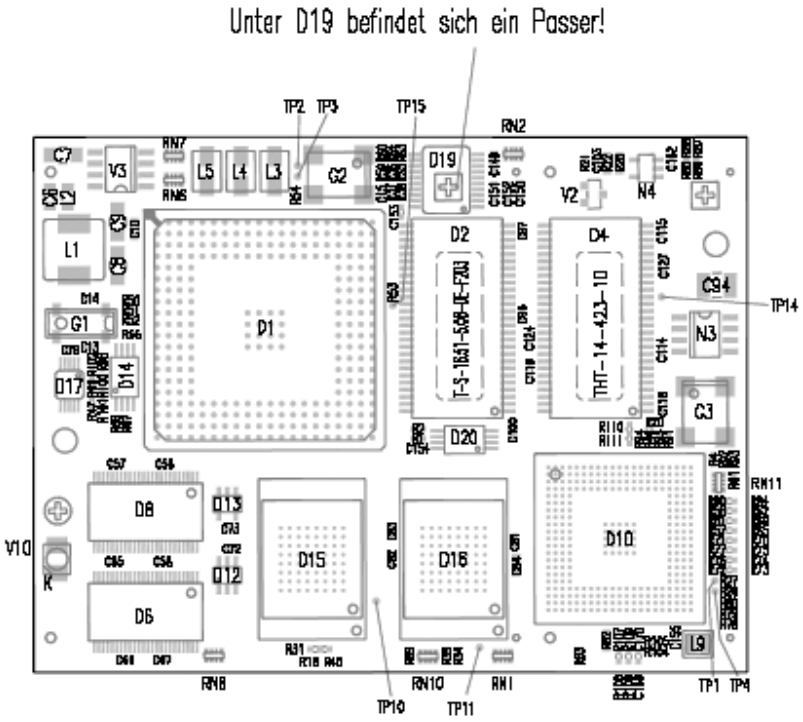


Illustration 10: View of the assembly side

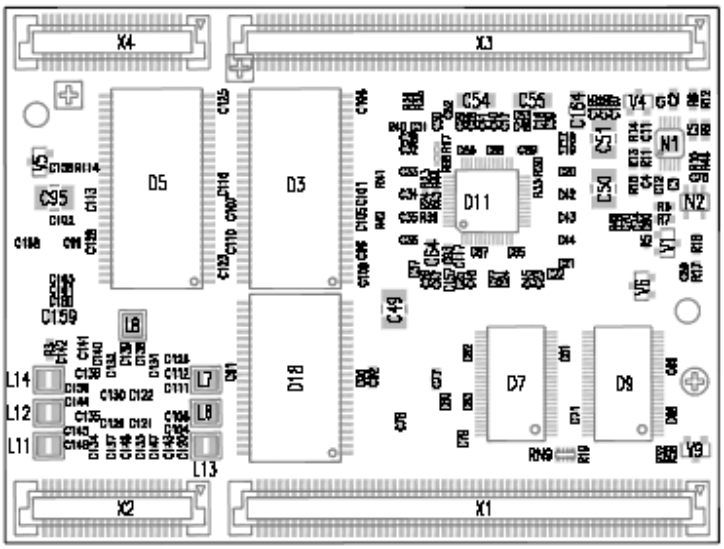


Illustration 11: View of the soldering side

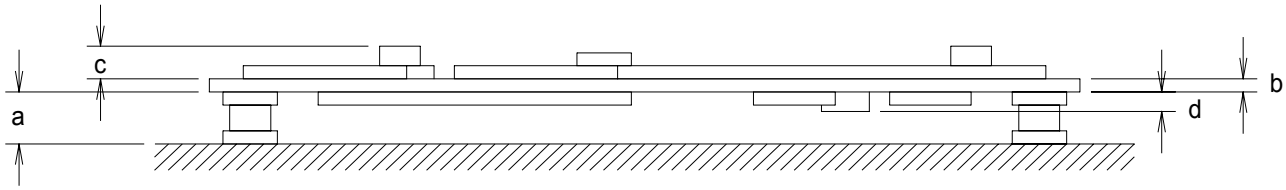


Illustration 12: Size (no scale)

Table 25: Size

Size	Value [mm]	Remark
a	5.0 ± 0.2	Combination Module connector with a counter piece of 6, 7 and 8 mm are also possible with another connector on the basis circuit.
b	1.8 ± 0.16	Printed circuit board
c	3.0 max.	Choke(Biggest size of the upper side)
d	1.6 max.	Kerko

5 SAFETY REQUIREMENTS AND PROTECTION STIPULATIONS

5.1 EMV-Requirements

The Module is developed accurately according to the requirements of the electromagnetic compatibility (EMC – EMV in German). Depending on the Target system, screening measures can nevertheless become necessary, in order to ensure adherence to certain limit values for the overall system.

Following measures are suggested:

- Stable mass ratio (enough mass) on the conductor board.
- Good connection between the circuit board mass in the case of metal housing. (at least HF-temperate) Connecting the circuit board mass to the housing potential.
- Enough block condensors on all the supply voltage
- Fast or continuously pulsating connections (e.g. Clock); Avoid interference in other signals by distancing or by electromagnetic shielding.
- Filtering of all the signals, which can be connected externally (even “slow” and same voltage signals can directly radiate HF)

5.2 ESD-Requirements

A good protection against electro magnetic discharge is attached directly at the input of the system. As these measures must always be realized on the basis circuit boards, no special protection measures are provided on TQM5200.

Following measures are suggested for a basis board:

- Generally applicable: Electro magnetic shielding of the supply line. (Massive Electro magnetic shielding on both sides connected to the mass/ housing).
- In the case of supply voltage: Protection by suppressor diodes.

- Slow signal lines: RC-Filtering , if required Z-Diode
- Fast signal lines : Integrated protective components (Suppressor diodes-Arrays)

5.3 Climate and installation conditions

Permissible ambient temperature: 0 .. +70°C, optional -40°C ..+85°C

Permissible storage temperature -5.. +85°C or. -55°C .. +100 °C

Protection class IP00 (No special protection against foreign bodies and humidity)

5.4 Reliability and lifespan

The typical lifespan of a module is 10 years. Vibration and stroke insensitive machines should be used.

5.5 Mechanism

	In order to avoid damages due to mechanical stress, the TQM must be removed from the basis circuit board only with the help of the drawing tool MOZI52xx.
	In order to be able to use the module drawing tool with the serial board, appropriate marked areas must be considered in the layout during realization.

Two drill holes are provided for fixing the module with the Basis hardware or for mounting the CPU heat sink.

6 APPENDIX

6.1 References

[1] MPC5200 Hardware Specifications; Rev.2 5/2004; Freescale

[2] MPC5200 Users Guide; Rev.2 8/2004; Freescale

[3] Application Note AN2458/D; Rev. 2 08/2004 (MPC5200 Local Plus Bus Interface) Freescale

[4] SM501_MMCC_Databook Rev.1.01; Silicon Motion

[5] Am29LV256ML
256 Megabit (16 M x 16-Bit/32 M x 8-Bit) MirrorBit™ 3.0 Volt-only Uniform Sector Flash Memory with VersatileI/O™ Control
Publication #25263 Rev. C Amendment /+2, Issue Date June 11, 2003

[6] MPC5200 (L25R) Errata; Rev.4 9/2004; Freescale

Notes