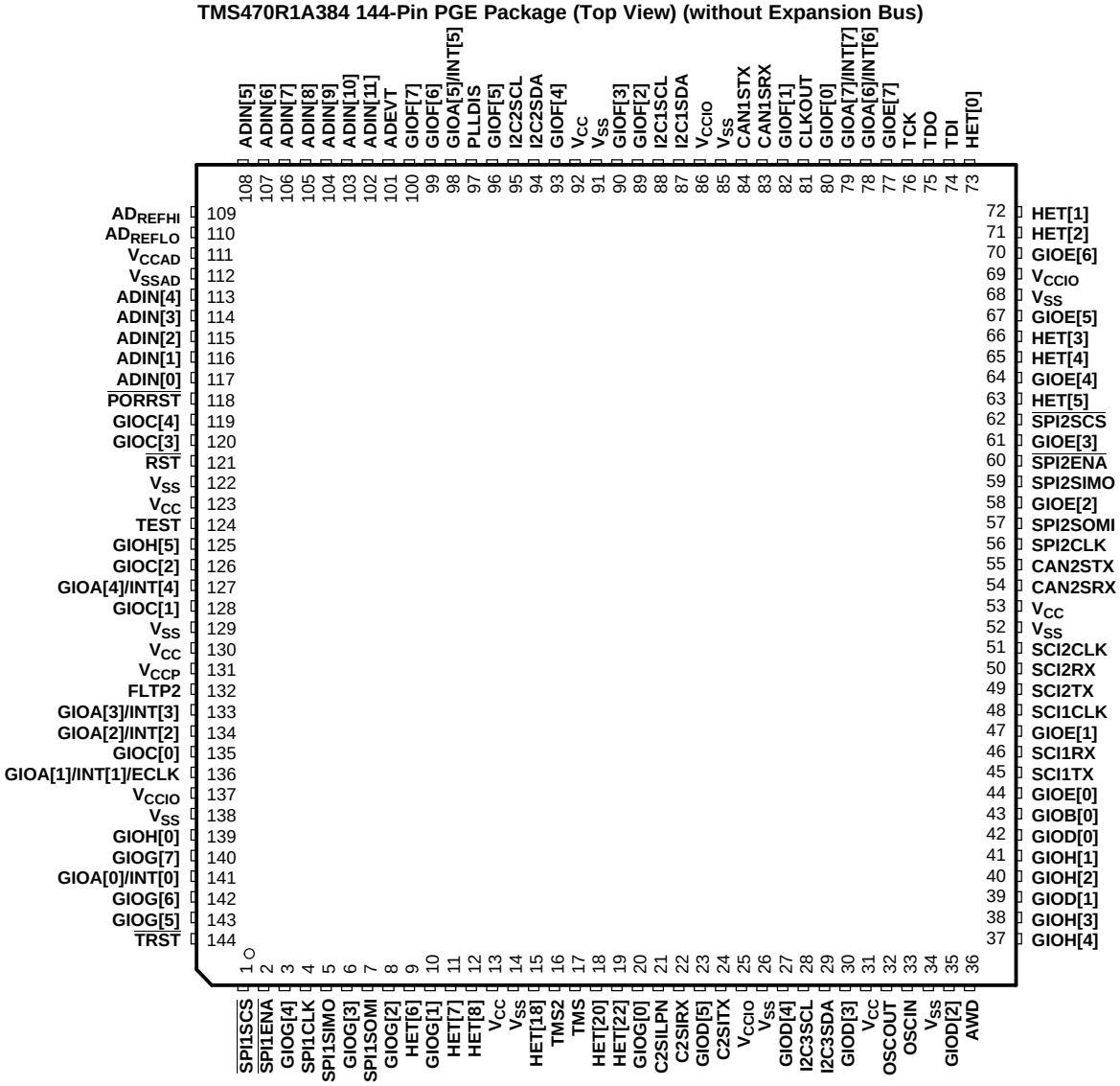
FEATURES

- High-Performance Static CMOS Technology
- TMS470R1x 16/32-Bit RISC Core (ARM7TDMI™)
  - 24-MHz System Clock (48-MHz Pipeline)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
- Integrated Memory
  - 384K-Byte Program Flash
    - Three Banks With 18 Contiguous Sectors
  - 32K-Byte Static RAM (SRAM)
- Operating Features
  - Core Supply Voltage (V_{CC}): 1.71 V–2.05 V
  - I/O Supply Voltage (V_{CCIO}): 3.0 V–3.6 V
  - Low-Power Modes: STANDBY and HALT
  - Extended Industrial Temperature Range
- 470+ System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory/Peripherals
  - Analog Watchdog (AWD) Timer
  - Enhanced Real-Time Interrupt (RTI)
  - Interrupt Expansion Module (IEM)
  - System Integrity and Failure Detection
- Direct Memory Access (DMA) Controller
  - 32 Control Packets and 16 Channels
- Zero-Pin Phase-Locked Loop (ZPLL)-Based Clock Module With Prescaler
  - Multiply-by-4 or -8 Internal ZPLL Option
  - ZPLL Bypass Mode
- Expansion Bus Module (EBM) (PGE Package only)
  - Supports 8- and 16-Bit Expansion Bus Memory Interface Mappings
  - 40 I/O Expansion Bus Pins
- Ten Communication Interfaces:
  - Two Serial Peripheral Interfaces (SPIs)
    - 255 Programmable Baud Rates
  - Two Serial Communication Interfaces (SCIs)
    - 2^{24} Selectable Baud Rates
    - Asynchronous/Isosynchronous Modes
  - Two Standard CAN Controllers (SCC)
    - 16-Mailbox Capacity
    - Fully Compliant With CAN Protocol, Version 2.0B
  - Class II Serial Interface B (C2SIb)
    - Normal 10.4 Kbps and 4X Mode 41.6 Kbps
  - Three Inter-Integrated Circuit (I2C) Modules
    - Multi-Master and Slave Interfaces
    - Up to 400 Kbps (Fast Mode)
    - 7- and 10-Bit Address Capability
- High-End Timer (HET)
  - 12 Programmable I/O Channels:
    - 12 High-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 64-Instruction Capacity
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (CLK)
- 12-Channel 10-Bit Multi-Buffered ADC (MibADC)
  - 32-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 µs Minimum Sample/Conversion Time
  - Calibration Mode and Self-Test Features
- 55 Dedicated General-Purpose I/O (GIO) Pins and 39 Additional Peripheral I/Os (PGE)
- 14 Dedicated General-Purpose I/O (GIO) Pins and 39 Additional Peripheral I/Os (PZ)
- Flexible Interrupt Handling
- 8 External Interrupts
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1[(1)] (JTAG) Test-Access Port
- 144-Pin Plastic Low-Profile Quad Flatpack (PGE Suffix)

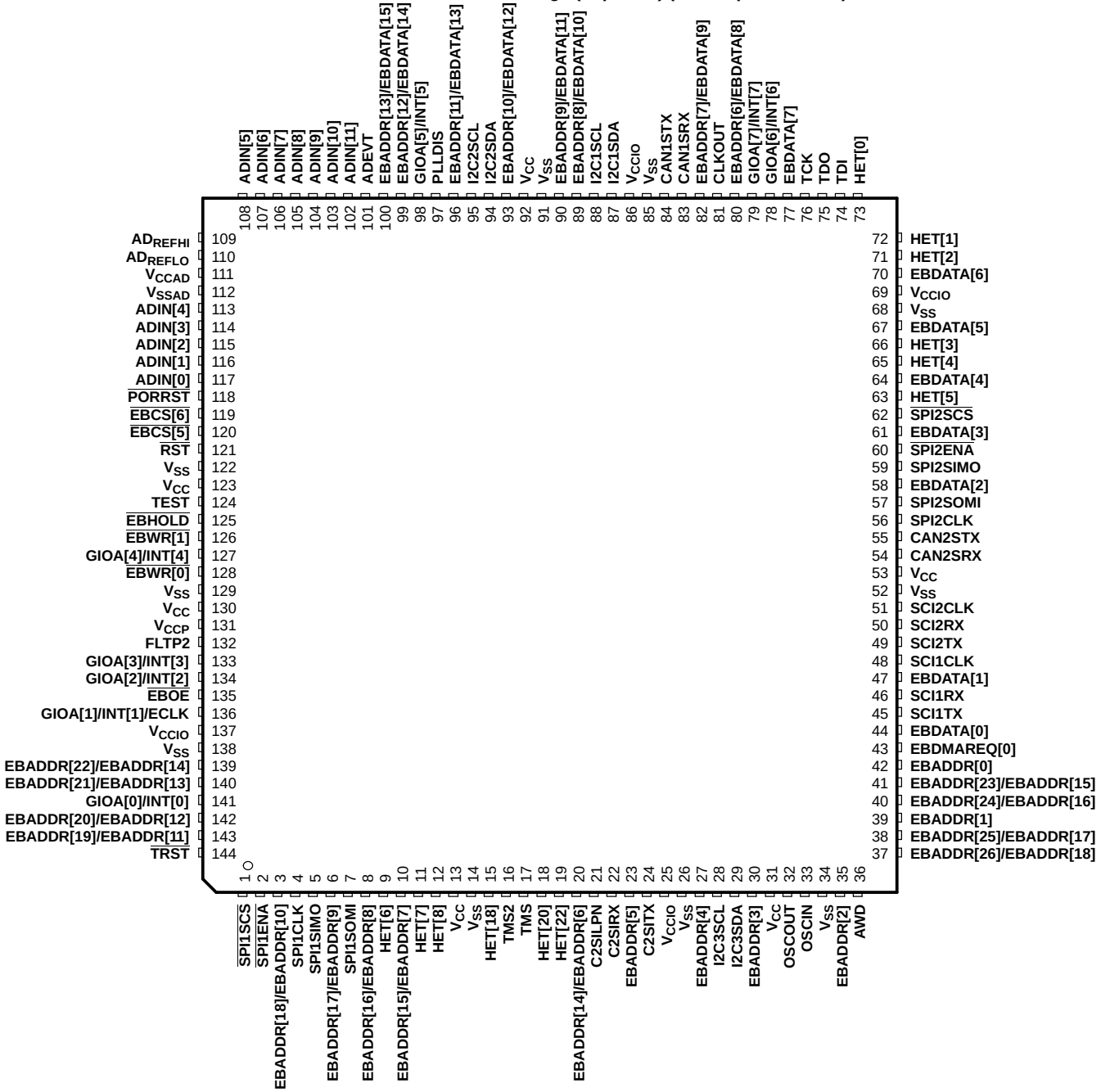
- **100-Pin Plastic Low-Profile Quad Flatpack (PZ Suffix)**

(1) The test-access port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

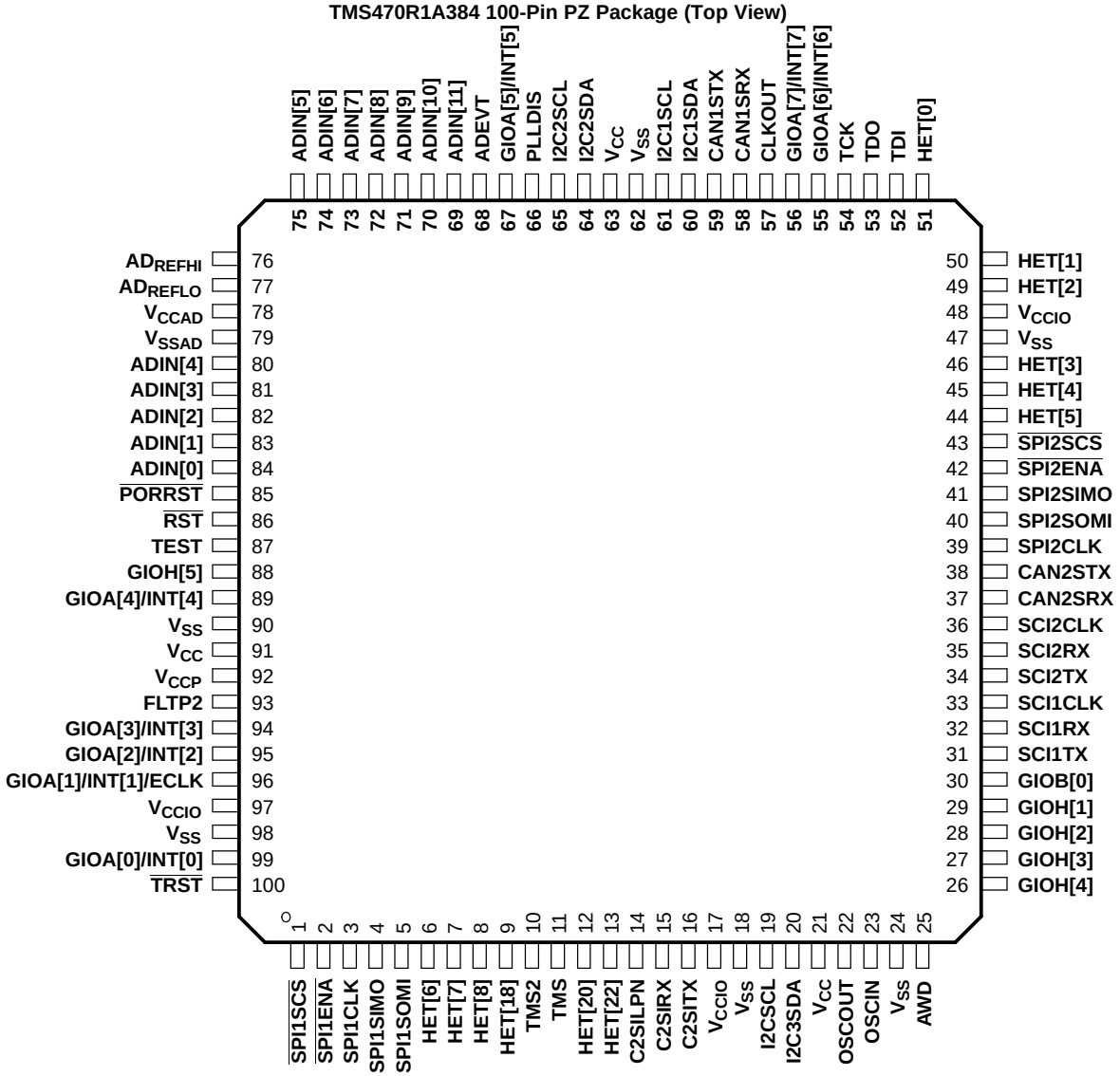
TMS470R1A384 144-Pin PGE Package (Top View) (without Expansion Bus)



TMS470R1A384 144-Pin PGE Package (Top View) (with Expansion Bus)



TMS470R1A384 100-Pin PZ Package (Top View)



DESCRIPTION

The TMS470R1A384(1) devices are members of the Texas Instruments TMS470R1x family of general-purpose 16/32-bit reduced instruction set computer (RISC) microcontrollers. The A384 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The A384 utilizes the big-endian format where the most significant byte of a word is stored at the lowest-numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The A384 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The A384 devices contain the following:

- ARM7TDMI 16/32-Bit RISC CPU
- TMS470R1x system module (SYS) with 470+ enhancements
- 384K-byte flash
- 32K-byte SRAM
- Zero-pin phase-locked loop (ZPLL) clock module
- Digital watchdog (DWD) timer
- Analog watchdog (AWD) timer
- Enhanced real-time interrupt (RTI) module
- Interrupt expansion module (IEM)
- Two serial peripheral interface (SPI) modules
- Two serial communications interface (SCI) modules
- Two standard CAN controllers (SCC)
- Three inter-integrated circuit (I2C) modules
- Class II serial interface B (C2SIb) module
- 10-bit multi-buffered analog-to-digital converter (MibADC), with 12 input channels
- High-end timer (HET) controlling 12 I/Os
- External clock prescale (ECP)
- Expansion bus module (EBM)
- Up to 87 I/O pins and 1 input-only pin (PGE suffix only), up to 51 I/O pins and 1 input-only pin (PZ suffix only)

The functions performed by the 470+ system module (SYS) include:

- Address decoding
- Memory protection
- Memory and peripherals bus supervision
- Reset and abort exception management
- Prioritization for all internal interrupt sources
- Device clock control
- Parallel signature analysis (PSA)

The enhanced real-time interrupt (RTI) module on the A384 has the option to be driven by the oscillator clock. The digital watchdog (DWD) is a 25-bit resettable decrementing counter that provides a system reset when the watchdog counter expires. This data sheet includes device-specific information such as memory and peripheral select assignment, interrupt priority, and a device memory map. For a more detailed functional description of the SYS module, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

The A384 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

(1) Throughout the remainder of this document, the TMS470R1A384 will be referred to as either the full device name or as A384.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The flash operates with a system clock frequency of up to 24 MHz. When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. For more detailed information on the flash, see the *Flash* section of this data sheet and the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

The A384 device has ten communication interfaces: two SPIs, two SCIs, two SCCs, a C2SI, and three I2Cs. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The SCI is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The SCC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The SCC is ideal for applications operating in noisy and harsh environments (e.g., industrial fields) that require reliable serial communication or multiplexed wiring. The C2SIb allows the A384 to transmit and receive messages on a class II network following an SAE J1850(2) standard. The I2C module is a multi-master communication module providing an interface between the A384 microcontroller and an I2C-compatible device via the I2C serial bus. The I2C supports both 100 Kbps and 400 Kbps speeds. For more detailed functional information on the SPI, SCI, and CAN peripherals, see the specific reference guides (literature numbers SPNU195, SPNU196, and SPNU197). For more detailed functional information on the I2C, see the *TMS470R1x Inter-Integrated Circuit (I2C) Reference Guide* (literature number SPNU223). For more detailed functional information on the C2SI, see the *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214).

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. The HET used in this device is the high-end timer lite. It has fewer I/Os than the usual 32 in a standard HET. For more detailed functional information on the HET, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The A384 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET. For more detailed information on the HET XOR-share feature, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).

The A384 device has one 10-bit-resolution, sample-and-hold MibADC. Each of the MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings, two of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode. For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

The zero-pin phase-locked loop (ZPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the ZPLL is to multiply the external frequency reference to a higher frequency for internal use. The ZPLL provides ACLK to the system (SYS) module. The SYS module subsequently provides system clock (SYSCLK), real-time interrupt clock (RTICLK), CPU clock (MCLK), and peripheral interface clock (ICLK) to all other A384 device modules. For more detailed functional information on the ZPLL, see the *TMS470R1x Zero Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212).

NOTE:

ACLK should not be confused with the MibADC internal clock, ADCLK. ACLK is the continuous system clock from an external resonator/crystal reference.

The expansion bus module (EBM) is a standalone module that supports the multiplexing of the GIO functions and the expansion bus interface. For more information on the EBM, see the *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222).

(2) SAE Standard J1850 Class B Data Communication Network Interface.

The A384 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK) on a specified GIO pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (ICLK) frequency. For more detailed functional information on the ECP, see the *TMS470R1x External Clock Prescaler (ECP) Reference Guide* (literature number SPNU202).

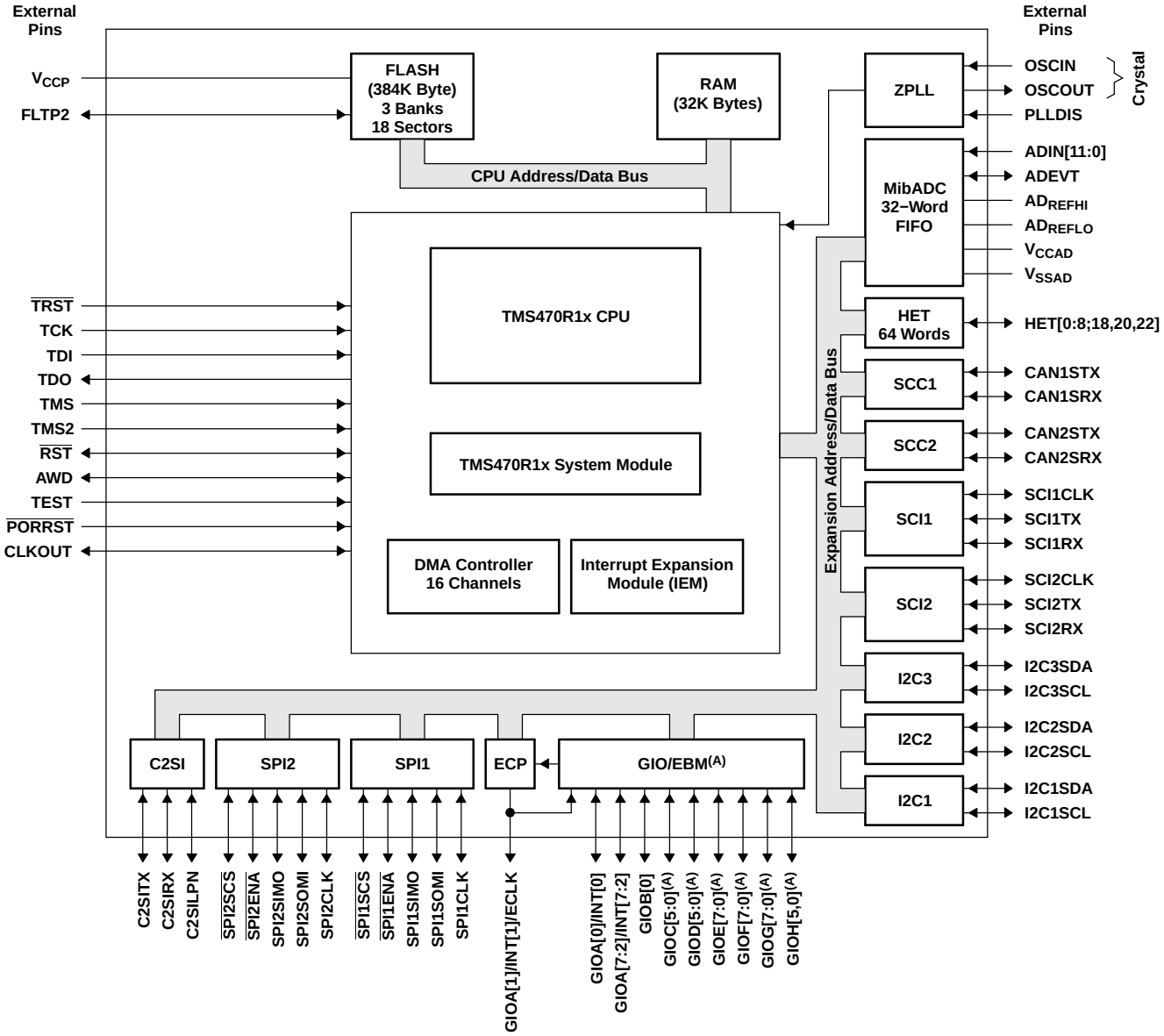
Device Characteristics

The A384 device is a derivative of the F05 system emulation device SE470R1VB8AD. Table 1 identifies all the characteristics of the A384 device except the SYSTEM and CPU, which are generic.

Table 1. Device Characteristics

CHARACTERISTICS	DEVICE DESCRIPTION TMS470R1A384	COMMENTS
MEMORY		
For the number of memory selects on this device, see Table 3, *TMS470R1A384 Memory Selection Assignment*.		
INTERNAL MEMORY	Pipeline/Non-Pipeline 384K-Byte Flash 32K-Byte SRAM	Flash is pipeline-capable. The A384 RAM is implemented in one 16K-byte array selected by two memory-select signals (see Table 3, *TMS470R1A384 Memory Selection Assignment*).
PERIPHERALS		
For the device-specific interrupt priority configurations, see Table 6, *Interrupt Priority (IEM and CIM)*. For the 1K-byte peripheral address ranges and their peripheral selects, see Table 4, *A384 Peripherals, System Module, and Flash Base Addresses*.		
CLOCK	ZPLL	Zero-pin PLL has no external loop filter pins.
Expansion Bus	EBM	Expansion bus module with 40 pins. Supports 8- and 16-bit memories, PGE package only. See Table 7 for details.
GENERAL-PURPOSE I/Os	55 I/O (PGE Suffix) 14 I/O (PZ Suffix)	In the PGE package, Port A has 8 external pins; Port B has only 1 external pin; Ports C, D, E, F, and G each have 8 external pins; and Port H has 6 external pins. In the PZ package, Port A has 8 external pins, Port B has 1 external pin, and Port H has 5 external pins.
ECP	YES	
SCI	2 (3-pin)	
CAN (HECC and/or SCC)	2 SCC	Two standard CAN controllers
SPI (5-pin, 4-pin or 3-pin)	2 (5-pin)	
C2SIb	1	
I2C	3	
HET with XOR Share	12 I/O	The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET RAM	64-Instruction Capacity	
MibADC	10-bit, 12-channel 64-word FIFO	Both the logic and registers for a full 16-channel MibADC are present.
CORE VOLTAGE	1.8 V	
I/O VOLTAGE	3.3 V	
PINS	144/100	
PACKAGES	PGE/PZ	

Functional Block Diagram



A. GIOC[4:0], GIOD[5:0], GIOE[5:0], GIOF[7:0], and GIOH[0], which are muxed with EBM, are not available on the PZ package. See Table 7 for EBM-to-GIO mapping.

Table 2. Terminal Functions

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(3)	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
HIGH-END TIMER (HET)						
HET[0]	51	73	3.3-V	2 mA		Timer input capture or output compare. The HET[8:0,18,20,22] applicable pins can be programmed as general-purpose input/output (GIO) pins. All are high-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. For more information on HR SHARE, see the *TMS470R1x High-End Timer (HET) Reference Guide* (literature number SPNU199).
HET[1]	50	72				
HET[2]	49	71				
HET[3]	46	66				
HET[4]	45	65				
HET[5]	44	63				
HET[6]	6	9				
HET[7]	7	11				
HET[8]	8	12				
HET[18]	9	15				
HET[20]	12	18				
HET[22]	13	19				
STANDARD CAN CONTROLLER (SCC)						
CAN1SRX	58	83	5 V tolerant	4 mA		SCC1 receive pin or GIO pin
CAN1STX	59	84	3.3-V	2 mA		SCC1 transmit pin or GIO pin
CAN2SRX	37	54	5 V tolerant	4 mA		SCC2 receive pin or GIO pin
CAN2STX	38	55	3.3-V	2 mA		SCC 2 transmit pin or GIO pin
CLASS II SERIAL INTERFACE (C2SIB)						
C2SILPN	14	21	3.3-V	2 mA		C2SIb module loopback enable pin or GIO pin
C2SIRX	15	22	5 V tolerant	4 mA		C2SIb module receive data input pin or GIO pin
C2SITX	16	24	3.3-V	2 mA		C2SIb module transmit data output pin or GIO pin
GENERAL-PURPOSE I/O (GIO)						
GIOA[0]/INT[0]	99	141	5 V tolerant	4 mA		General-purpose input/output pins. GIOA[7:0]/INT[7:0] are interrupt-capable pins. GIOA[1]/INT[1]/ECLK pin is multiplexed with the external clock-out function of the external clock prescale (ECP) module.
GIOA[1]/INT[1]/ECLK	96	136				
GIOA[2]/INT[2]	95	134				
GIOA[3]/INT[3]	94	133				
GIOA[4]/INT[4]	89	127				
GIOA[5]/INT[5]	67	98				
GIOA[6]/INT[6]	55	78				
GIOA[7]/INT[7]	56	79				
GIOB[0]/DMAREQ[0]	30	43	3.3-V	2 mA	IPD (20 µA)	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], and GIOH[5:0] are multiplexed with the expansion bus module. See Table 7.
GIOC[0]/$\overline{\text{EBOE}}$	-	135				
GIOC[1]/$\overline{\text{EBWR}}$[0]	-	128				
GIOC[2]/$\overline{\text{EBWR}}$[1]	-	126				
GIOC[3]/$\overline{\text{EBCS}}$[5]	-	120				
GIOC[4]/$\overline{\text{EBCS}}$[6]	-	119				

(1) PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.)

Table 2. Terminal Functions (continued)

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(3)	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
GENERAL-PURPOSE I/O (GIO) (CONTINUED)						
GIOD[0]/EBADDR[0]	-	42	3.3-V	2 mA	IPD (20 µA)	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], AND GIOH[5:0] are multiplexed with the expansion bus module. See Table 7.
GIOD[1]/EBADDR[1]	-	39				
GIOD[2]/EBADDR[2]	-	35				
GIOD[3]/EBADDR[3]	-	30				
GIOD[4]/EBADDR[4]	-	27				
GIOD[5]/EBADDR[5]	-	23				
GIOE[0]/EBDATA[0]	-	44				
GIOE[1]/EBDATA[1]	-	47				
GIOE[2]/EBDATA[2]	-	58				
GIOE[3]/EBDATA[3]	-	61				
GIOE[4]/EBDATA[4]	-	64				
GIOE[5]/EBDATA[5]	-	67				
GIOE[6]/EBDATA[6]	-	70				
GIOE[7]/EBDATA[7]	-	77				
GIOF[0]/EBADDR[6]/ EBDATA[8]	-	80				
GIOF[1]/EBADDR[7]/ EBDATA[9]	-	82				
GIOF[2]/EBADDR[8]/ EBDATA[10]	-	89				
GIOF[3]/EBADDR[9]/ EBDATA[11]	-	90				
GIOF[4]/EBADDR[10] /EBDATA[12]	-	93				
GIOF[5]/EBADDR[11] /EBDATA[13]	-	96				
GIOF[6]/EBADDR[12] /EBDATA[14]	-	99				
GIOF[7]/EBADDR[13] /EBDATA[15]	-	100				
GIOG[0]/EBADDR[14] /EBADDR[6]	-	20				
GIOG[1]/EBADDR[15] /EBADDR[7]	-	10				
GIOG[2]/EBADDR[16] /EBADDR[8]	-	8				
GIOG[3]/EBADDR[17] /EBADDR[9]	-	6				

Table 2. Terminal Functions (continued)

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(3)	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
GENERAL-PURPOSE I/O (GIO) (CONTINUED)						
GIOG[4]/EBADDR[18] /EBADDR[10]	-	3	3.3-V	2 mA	IPD (20 µA)	GIOB[0], GIOC[4:0], GIOD[5:0], GIOE[7:0:], GIOF[7:0], GIOG[7:0], AND GIOH[5:0] are multiplexed with the expansion bus module. See Table 7. GIOH[5:0]/INT[13:8] are interrupt-capable pins.
GIOG[5]/EBADDR[19] /EBADDR[11]	-	143				
GIOG[6]/EBADDR[20] /EBADDR[12]	-	142				
GIOG[7]/EBADDR[21] /EBADDR[13]	-	140				
GIOH[0]/EBADDR[22] /EBADDR[14]	-	139				
GIOH[1]/EBADDR[23] /EBADDR[15]	29	41				
GIOH[2]/EBADDR[24] /EBADDR[16]	28	40				
GIOH[3]/EBADDR[25] /EBADDR[17]	27	38				
GIOH[4]/EBADDR[26] /EBADDR[18]	26	37				
GIOH[5]/$\overline{\text{EBHOLD}}$	88	125				
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)						
ADEVT	68	101	3.3-V	2 mA		MibADC event input. Can be programmed as a GIO pin.
ADIN[0]	84	117	3.3-V			MibADC analog input pins
ADIN[1]	83	116				
ADIN[2]	82	115				
ADIN[3]	81	114				
ADIN[4]	80	113				
ADIN[5]	75	108				
ADIN[6]	74	107				
ADIN[7]	73	106				
ADIN[8]	72	105				
ADIN[9]	71	104				
ADIN[10]	70	103				
ADIN[11]	69	102				
AD_{REFHI}	76	109	3.3-V REF			MibADC module high-voltage reference input
AD_{REFLO}	77	110	GND REF			MibADC module low-voltage reference input
V_{CCAD}	78	111	3.3-V PWR			MibADC analog supply voltage
V_{SSAD}	79	112	GND			MibADC analog ground reference

Table 2. Terminal Functions (continued)

TERMINAL			INPUT VOLTAGE[1][2]	OUTPUT CURRENT[3]	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
SERIAL PERIPHERAL INTERFACE 1 (SPI1)						
SPI1CLK	3	4	5 V tolerant	4 mA		SPI1 clock. SPI1CLK can be programmed as a GIO pin.
$\overline{\text{SPI1ENA}}$	2	2				SPI1 chip enable. Can be programmed as a GIO pin.
$\overline{\text{SPI1SCS}}$	1	1				SPI1 slave chip select. Can be programmed as a GIO pin.
SPI1SIMO	4	5				SPI1 data stream. Slave in/master out. Can be programmed as a GIO pin.
SPI1SOMI	5	7				SPI1 data stream. Slave out/master in. Can be programmed as a GIO pin.
SERIAL PERIPHERAL INTERFACE 2 (SPI2)						
SPI2CLK	39	56	5 V tolerant	4 mA		SPI2 clock. Can be programmed as a GIO pin.
$\overline{\text{SPI2ENA}}$	42	60				SPI2 chip enable. Can be programmed as a GIO pin.
$\overline{\text{SPI2SCS}}$	43	62				SPI2 slave chip select. Can be programmed as a GIO pin.
SPI2SIMO	41	59				SPI2 data stream. Slave in/master out. Can be programmed as a GIO pin.
SPI2SOMI	40	57				SPI2 data stream. Slave out/master in. Can be programmed as a GIO pin.
INTER-INTEGRATED CIRCUIT (I2C)						
I2C1SDA	60	87	5 V tolerant	4 mA		I2C1 serial data pin or GIO pin
I2C1SCL	61	88				I2C1 serial clock pin or GIO pin
I2C2SDA	64	94				I2C2 serial data pin or GIO pin
I2C2SCL	65	95				I2C2 serial clock pin or GIO pin
I2C3SDA	20	29				I2C3 serial data pin or GIO pin
I2C3SCL	19	28				I2C3 serial clock pin or GIO pin
ZERO-PIN PHASE-LOCKED LOOP (ZPLL)						
OSCIN	23	33	1.8-V			Crystal connection pin or external clock input
OSCOUT	22	32		2 mA		External crystal connection pin
PLLDIS	66	97	3.3-V		IPD (20 µA)	Enable/disable the ZPLL. The ZPLL can be bypassed and the oscillator becomes the system clock.
SERIAL COMMUNICATIONS INTERFACE 1 (SCI1)						
SCI1CLK	33	48	3.3-V	2 mA		SCI1 clock. SCI1CLK can be programmed as a GIO pin.
SCI1RX	32	46	5 V tolerant	4 mA		SCI1 data receive. SCI1RX can be programmed as a GIO pin.
SCI1TX	31	45	3.3-V	2 mA		SCI1 data transmit. SCI1TX can be programmed as a GIO pin.
SERIAL COMMUNICATIONS INTERFACE 2 (SCI2)						
SCI2CLK	36	51	3.3-V	2 mA		SCI2 clock. SCI2CLK can be programmed as a GIO pin.
SCI2RX	35	50	5 V tolerant	4 mA		SCI2 data receive. SCI2RX can be programmed as a GIO pin.
SCI2TX	34	49	3.3-V	2 mA		SCI2 data transmit. SCI2TX can be programmed as a GIO pin.

Table 2. Terminal Functions (continued)

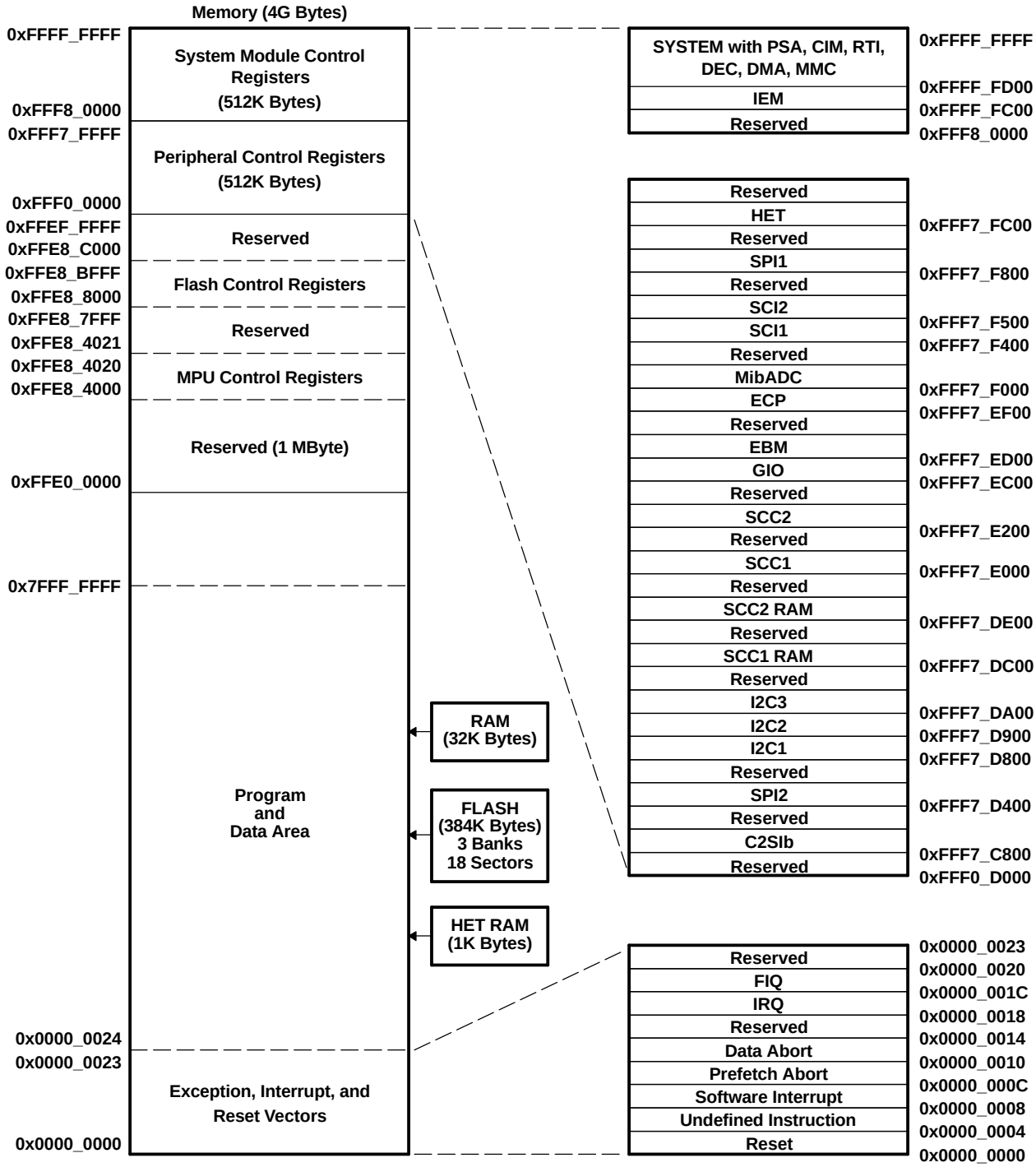
TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(3)	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
SYSTEM MODULE (SYS)						
CLKOUT	57	81	3.3-V	4 mA		Bidirectional pin. CLKOUT can be programmed as a GIO pin or the output of SYSCLK, ICLK, or MCLK.
$\overline{\text{PORRST}}$	85	118	3.3-V		IPD (20 µA)	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	86	121	3.3-V	4 mA	IPU (20 µA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)						
AWD	25	36	3.3-V	8 mA		Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. For more details on the external RC network circuit, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
TEST/DEBUG (T/D)						
TCK	54	76	3.3-V	2 mA	IPD (20 µA)	Test clock. TCK controls the test hardware (JTAG).
TDI	52	74		2 mA		Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	53	75		4 mA		Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TEST	87	124				Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
TMS	11	17		2 mA		Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG).
TMS2	10	16		2 mA		Serial input for controlling the second TAP. TI recommends that this pin be connected to V_{CCIO} or pulled up to V_{CCIO} by an external resistor.
$\overline{\text{TRST}}$	100	144				Test hardware reset to TAP1 and TAP2. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. TI recommends that this pin be pulled down to ground by an external resistor.

Table 2. Terminal Functions (continued)

TERMINAL			INPUT VOLTAGE(1)(2)	OUTPUT CURRENT(3)	INTERNAL PULLUP/ PULLDOWN	DESCRIPTION
NAME	PZ	PGE				
FLASH						
FLTP2	93	132	NC	NC		Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].**
V_{CCP}	92	131	3.3-V PWR			Flash external pump voltage (3.3 V)
SUPPLY VOLTAGE CORE (1.8 V)						
V_{CC}	21	13	1.8-V	PWR		Core logic supply voltage
	63	31				
	91	53				
	-	92				
	-	123				
	-	130				
SUPPLY VOLTAGE DIGITAL I/O (3.3 V)						
V_{CCIO}	17	25	3.3-V	PWR		Digital I/O supply voltage
	48	69				
	-	86				
	97	137				
SUPPLY GROUND CORE						
V_{SS}	90	14	GND			Core supply ground reference
	98	26				
	-	34				
	-	52				
	-	68				
	47	85				
	-	91				
	62	122				
	24	129				
	18	138				

TMS470R1A384 DEVICE-SPECIFIC INFORMATION

Memory



A. Memory addresses are configurable by the system (SYS) module within the range of 0x0000_0000 to 0xFFE0_0000.

B. The CPU registers are not a part of the memory map.

Figure 1. TMS470R1A384 Memory Map

Memory Selects

Memory selects allow the user to address memory arrays (i.e., flash, RAM, and HET RAM) at user-defined addresses. Each memory select has its own set (low and high) of memory base address registers (MFBAHRx and MFBALRx) that, together, define the array's starting (base) address, block size, and protection.

The base address of each memory select is configurable to any memory address boundary that is a multiple of the decoded block size. For more information on how to control and configure these memory select registers, see the bus structure and memory sections of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

For the memory selection assignments and the memory selected, see Table 3.

Table 3. TMS470R1A384 Memory Selection Assignment

MEMORY SELECT	MEMORY SELECTED (ALL INTERNAL)	MEMORY SIZE(1)	MPU	MEMORY BASE ADDRESS REGISTER	STATIC MEM CTL REGISTER
0 (fine)	FLASH	384K	NO	MFBAHR0 and MFBALR0	
1 (fine)	FLASH		NO	MFBAHR1 and MFBALR1	
2 (fine)	RAM	32K(2)	YES	MFBAHR2 and MFBALR2	
3 (fine)	RAM		YES	MFBAHR3 and MFBALR3	
4 (fine)	HET RAM	1K	NO	MFBAHR4 and MFBALR4	SMCR1
5 (fine)	$\overline{\text{CS}}$[5]/GIOC[3]	4MB (x8) 1MB (x16)	NO	MCBAHR2 and MCBALR2	SMCR5
6 (fine)	$\overline{\text{CS}}$[6]/GIOC[4]	4MB (x8) 1MB (x16)	NO	MCBAHR3 and MCBALR3	SMCR6

(1) x8 refers to size of memory in 8-bits; x16 refers to size of memory in 16-bits.
(2) The starting addresses for both RAM memory-select signals cannot be offset from each other by a multiple of the user-defined block size in the memory-base address register.

RAM

The A384 device contains 32K-bytes of internal static RAM configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. This A384 RAM is implemented in one 32K-byte array selected by two memory-select signals.

NOTE:

This A384 configuration imposes an additional constraint on the memory map for RAM; the starting addresses for both RAM memory selects cannot be offset from each other by the multiples of the size of the physical RAM (i.e., 32K bytes for the A384 device). The A384 RAM is addressed through memory selects 2 and 3.

The RAM can be protected by the memory protection unit (MPU) portion of the SYS module, allowing the user finer blocks of memory protection than is allowed by the memory selects. The MPU is ideal for protecting an operating system while allowing access to the current task. For more detailed information on the MPU portion of the SYS module and memory protection, see the memory section of the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

F05 Flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions. See the *Flash Read* and *Flash Program and Erase* sections below.

Flash Protection Keys

The A384 device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the A384 are located in the last 4 words of the first 8K sector. For more detailed information on the flash protection keys and the FMPKEY control register, see the "Optional Quadruple Protection Keys" and "Programming the Protection Keys" portions of the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

Flash Read

The A384 flash memory is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The flash is addressed through memory selects 0 and 1.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Flash Pipeline Mode

When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz (versus a system clock frequency of 24 MHz in normal mode). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also, in pipeline mode the flash can be read with no wait states when memory addresses are contiguous (after the initial 1- or 2-wait-state reads).

NOTE:

After a system reset, pipeline mode is disabled (FMREGOPT[0] = 0). In other words, the A384 device powers up and comes out of reset in non-pipeline mode. Furthermore, setting the flash configuration mode bit (GBLCTRL[4]) will override pipeline mode.

Flash Program and Erase

The A384 device flash contains three 128K-byte memory arrays (or banks), for a total of 384K-bytes of flash, and consists of eighteen sectors. These eighteen sectors are sized as follows:

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	8K Bytes	0x0000_0000	0x0000_1FFF	BANK0 (128K Bytes)
1	8K Bytes	0x0000_2000	0x0000_3FFF	
2	16K Bytes	0x0000_4000	0x0000_7FFF	
3	16K Bytes	0x0000_8000	0x0000_BFFF	
4	16K Bytes	0x0000_C000	0x0000_FFFF	
5	16K Bytes	0x0001_0000	0x0001_3FFF	
6	16K Bytes	0x0001_4000	0x0001_7FFF	
7	16K Bytes	0x0001_8000	0x0001_BFFF	
8	8K Bytes	0x0001_C000	0x0001_DFFF	
9	8K bytes	0x0001_E000	0x0001_FFFF	
0	32K Bytes	0x0002_0000	0x0002_7FFF	BANK1 (128K Bytes)
1	32K Bytes	0x0002_8000	0x0002_FFFF	
2	32K Bytes	0x0003_0000	0x0003_7FFF	
3	32K Bytes	0x0003_8000	0x0003_FFFF	
0	32K Bytes	0x0004_0000	0x0004_7FFF	BANK2 (128K Bytes)
1	32K Bytes	0x0004_8000	0x0004_FFFF	
2	32K Bytes	0x0005_0000	0x0005_7FFF	
3	32K Bytes	0x0005_8000	0x0005_FFFF	

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

NOTE:

The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).

Execution can occur from one bank while programming/erasing any or all sectors of another bank. However, execution cannot occur from any sector within a bank that is being programmed or erased.

NOTE:

When the OTP sector is enabled, the rest of the flash memory is disabled. The OTP memory can only be read or programmed from code executed out of RAM.

For more detailed information on flash program and erase operations, see the *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213).

HET RAM

The A384 device contains HET RAM. The HET RAM has a 64-instruction capability. The HET RAM is configurable by the SYS module to be addressed within the range of 0x0000_0000 to 0xFFE0_0000. The HET RAM is addressed through memory select 4.

Peripheral Selects and Base Addresses

The A384 device uses 10 of the 16 peripheral selects to decode the base addresses of the peripherals. These peripheral selects are fixed and transparent to the user because they are part of the decoding scheme used by the SYS module.

Control registers for the peripherals, SYS module, and flash begin at the base addresses shown in Table 4.

Table 4. A384 Peripherals, System Module, and Flash Base Addresses

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
SYSTEM	0xFFFF_FFCC	0x FFFF_FFFF	N/A
RESERVED	0xFFFF_FF60	0xFFFF_FFCB	N/A
PSA	0xFFFF_FF40	0xFFFF_FF5F	N/A
CIM	0xFFFF_FF20	0xFFFF_FF3F	N/A
RTI	0xFFFF_FF00	0xFFFF_FF1F	N/A
DMA	0xFFFF_FE80	0xFFFF_FEFF	N/A
DEC	0xFFFF_FE00	0xFFFF_FE7F	N/A
MMC	0xFFFF_FD00	0xFFFF_FD7F	N/A
IEM	0xFFFF_FC00	0xFFFF_FCFF	N/A
RESERVED	0xFFFF_FB00	0xFFFF_FBFF	N/A
RESERVED	0xFFFF_FA00	0xFFFF_FAFF	N/A
DMA CMD BUFFER	0xFFFF_F800	0xFFFF_F9FF	N/A
RESERVED	0xFFF8_0000	0xFFFF_F7FF	N/A
HET	0xFFF7_FC00	0xFFF7_FFFF	PS[0]
SPI1	0xFFF7_F800	0xFFF7_FBFF	PS[1]
SCI2	0XFFF7_F500	0XFFF7_F7FF	PS[2]
SCI1	0xFFF7_F400	0xFFF7_F4FF	
MibADC	0xFFF7_F000	0xFFF7_F3FF	PS[3]
ECP	0xFFF7_EF00	0xFFF7_EFFF	PS[4]
RESERVED	0xFFF7_EE00	0xFFF7_EEFF	
EBM	0xFFF7_ED00	0xFFF7_EDFF	
GIO	0xFFF7_EC00	0xFFF7_ECFF	
RESERVED	0xFFF7_E400	0xFFF7_EBFF	PS[5]–PS[6]
RESERVED	0xFFF7_E300	0xFFF7_E3FF	PS[7]
SCC2	0xFFF7_E200	0xFFF7_E2FF	
RESERVED	0xFFF7_E100	0xFFF7_E1FF	
SCC1	0xFFF7_E000	0xFFF7_E0FF	
RESERVED	0xFFF7_DF00	0xFFF7_DFFF	PS[8]
SCC2 RAM	0xFFF7_DE00	0xFFF7_DEFF	
RESERVED	0xFFF7_DD00	0xFFF7_DDFF	
SCC1 RAM	0xFFF7_DC00	0xFFF7_DCFF	
RESERVED	0xFFF7_DB00	0xFFF7_DBFF	PS[9]
I2C3	0xFFF7_DA00	0xFFF7_DAFF	
I2C2	0xFFF7_D900	0xFFF7_D9FF	
I2C1	0xFFF7_D800	0xFFF7_D8FF	
SPI2	0xFFF7_D400	0xFFF7_D7FF	PS[10]
RESERVED	0xFFF7_CC00	0xFFF7_D3FF	PS[11]–PS[12]
C2SIb	0xFFF7_C800	0xFFF7_CBFF	PS[13]
RESERVED	0xFFF7_C000	0xFFF7_C7FF	PS[14]–PS[15]
RESERVED	0xFFF0_0000	0xFFF7_BFFF	N/A
Flash Control Registers	0xFFE8_8000	0xFFE8_BFFF	N/A
MPU Control Registers	0xFFE8_4000	0xFFE8_4023	N/A

Direct-Memory Access (DMA)

The direct-memory access (DMA) controller transfers data to and from any specified location in the A384 memory map (except for restricted memory locations like the system control registers area). The DMA manages up to 16 channels, and supports data transfer for both on-chip and off-chip memories and peripherals. The DMA controller is connected to both the CPU and peripheral buses, enabling these data transfers to occur in parallel with CPU activity and thus maximizing overall system performance.

Although the DMA controller has two possible configurations for the A384 device, the DMA controller configuration is 32 control packets and 16 channels.

For the A384 DMA request hardwired configuration, see Table 5.

Table 5. DMA Request Lines Connections(1)

MODULES	DMA REQUEST INTERRUPT SOURCES		DMA CHANNEL
EBM	Expansion Bus DMA request	EBDMAREQ0	DMAREQ[0]
SPI1	SPI1 end-receive	SPI1DMA0	DMAREQ[1]
SPI1	SPI1 end-transmit	SPI1DMA1	DMAREQ[2]
I2C1	I2C1 read	I2C1DMA0	DMAREQ[3]
SCI1	SCI1 end-receive	SCI1DMA0	DMAREQ[4]
SCI1	SCI1 end-transmit	SCI1DMA1	DMAREQ[5]
I2C1	I2C1 write	I2C1DMA1	DMAREQ[6]
SPI2	SPI2 end-receive	SPI2DMA0	DMAREQ[7]
SPI2	SPI2 end-transmit	SPI2DMA1	DMAREQ[8]
I2C2/C2SIb	I2C2 read/C2SIb end-receive	I2C2DMA0/C2SIDMA0	DMAREQ[9]
I2C2/C2SIb	I2C2 write/C2SIb end-transmit	I2C2DMA1/C2SIDMA1	DMAREQ[10]
I2C3	I2C3 read	I2C3DMA0	DMAREQ[11]
I2C3	I2C3 write	I2C3DMA1	DMAREQ[12]
Reserved			DMAREQ[13]
SCI2/SPI3	SCI2 end-receive	SCI2DMA0	DMAREQ[14]
SCI2/SPI3	SCI2 end-transmit	SCI2DMA1	DMAREQ[15]

(1) For DMA channels with more than one assigned request source (I2C2/C2SIb), only one of the sources listed can be the DMA request generator in a given application. The device has software control to ensure that there are no conflicts between requesting modules.

Each channel has two control packets attached to it, allowing the DMA to continuously load RAM and generate periodic interrupts so that the data can be read by the CPU. The control packets allow for the interrupt enable, and the channels determine the priority level of the interrupt.

DMA transfers occur in one of two modes:

- Non-request mode (used when transferring from memory to memory)
- Request mode (used when transferring from memory to peripheral)

For more detailed functional information on the DMA controller, see the *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194).

Interrupt Priority (IEM to CIM)

Interrupt requests originating from the A384 peripheral modules (i.e., SPI1 or SPI2; SCI1 or SCI2; RTI; etc.) are assigned to channels within the 48-channel interrupt expansion module (IEM) where, via programmable register mapping, these channels are then mapped to the 32-channel central interrupt manager (CIM) portion of the SYS module.

Programming multiple interrupt sources in the IEM to the same CIM channel effectively shares the CIM channel between sources.

The CIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the CIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The CIM prioritizes interrupts. The precedences of request channels decrease with ascending channel order in the CIM (0 [highest] and 31 [lowest] priority). For IEM-to-CIM default mapping, channel priorities, and their associated modules, see Table 6.

Table 6. Interrupt Priority (IEM and CIM)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/CHANNEL	IEM CHANNEL
SPI1	SPI1 end-transfer/overrun	0	0
RTI	COMP2 interrupt	1	1
RTI	COMP1 interrupt	2	2
RTI	TAP interrupt	3	3
SPI2	SPI2 end-transfer/overrun	4	4
GIO	GIO interrupt A	5	5
Reserved		6	6
HET	HET interrupt 1	7	7
I2C1	I2C1 interrupt	8	8
SCI1/SCI2	SCI1 or SCI2 error interrupt	9	9
SCI1	SCI1 receive interrupt	10	10
C2SIb	C2SIb interrupt	11	11
I2C2	I2C2 interrupt	12	12
SCC2	SCC2 interrupt A	13	13
SCC1	SCC1 interrupt A	14	14
Reserved		15	15
MibADC	MibADC end event conversion	16	16
SCI2	SCI2 receive interrupt	17	17
DMA	DMA interrupt 0	18	18
I2C3	I2C3 interrupt	19	19
SCI1	SCI1 transmit interrupt	20	20
System	SW interrupt (SSI)	21	21
Reserved		22	22
HET	HET interrupt 2	23	23
SCC2	SCC2 interrupt B	24	24
SCC1	SCC1 interrupt B	25	25
SCI2	SCI2 transmit interrupt	26	26
MibADC	MibADC end group1 conversion	27	27
DMA	DMA Interrupt 1	28	28
GIO	GIO interrupt B	29	29
MibADC	MibADC end group2 conversion	30	30

Table 6. Interrupt Priority (IEM and CIM) (continued)

MODULES	INTERRUPT SOURCES	DEFAULT CIM INTERRUPT LEVEL/CHANNEL	IEM CHANNEL
Reserved		31	31
Reserved		31	32
Reserved		31	33
Reserved		31	34
Reserved		31	35
Reserved		31	36
Reserved		31	37
Reserved		31	38
Reserved		31	39
Reserved		31	40
Reserved		31	41
Reserved		31	42
Reserved		31	43
Reserved		31	44
Reserved		31	45
Reserved		31	46
Reserved		31	47

For more detailed functional information on the IEM, see the *TMS470R1x Interrupt Expansion Module (IEM) Reference Guide* (literature number SPNU211). For more detailed functional information on the CIM, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

Expansion Bus Module (EBM)

The expansion bus module (EBM) is a standalone module used to bond out both general-purpose input/output pins and expansion bus interface pins. The module supports 8- and 16-bit expansion bus memory interface mappings, as well as mapping of the following expansion bus signals:

- 22-bit address bus (EBADDR[21:0]) for x8, 19-bit address bus (EBADDR[18:0]) for x16
- 8- or 16-bit data bus (EBDATA[7:0]or EBDATA[15:0])
- 2 write strobes ($\overline{\text{EBWR}}$[1:0])
- 2 memory chip selects ($\overline{\text{EBCS}}$[6:5])
- 1 output enable ($\overline{\text{EBOE}}$)
- 1 external hold signal for interfacing to slow memories ($\overline{\text{EBHOLD}}$)

Table 7 shows the multiplexing of I/O signals with the expansion bus interface signals. The mapping of these pins varies depending on the memory mode.

Table 7. Expansion Bus Mux Mapping(1)

GIO	EXPANSION BUS MODULE PINS(2)	
	x8	x16
GIOB[0]	EBDMAREQ[0]	EBDMAREQ[0]
GIOC[0]	$\overline{\text{EBOE}}$	$\overline{\text{EBOE}}$
GIOC[2:1]	$\overline{\text{EBWR}}$[1:0]	$\overline{\text{EBWR}}$[1:0]
GIOC[4:3]	$\overline{\text{EBCS}}$[6:5]	$\overline{\text{EBCS}}$[6:5]
GIOD[5:0]	EBADDR[5:0]	EBADDR[5:0]
GIOE[7:0]	EBDATA[7:0]	EBDATA[7:0]
GIOF[7:0]	EBADDR[13:6]	EBDATA[15:8]
GIOG[7:0]	EBADDR[21:14]	EBADDR[13:6]
GIOH[4:0]	-	EBADDR[18:14]
GIOH[5]	$\overline{\text{EBHOLD}}$	$\overline{\text{EBHOLD}}$

(1) These mappings are controlled by the EBM mux control registers B–H (EBMXCRB–EBMXCRH) and the EBM control register 1 (EBMCR1). For GPIO functions, use GIODIRx, GIODINx, GIODOUTx, GIODSETx, and GIODCLRx. For more detailed information, see the *TMS470R1x General-Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192) and the *TMS470R1x Expansion Bus Module (EBM) Reference Guide* (literature number SPNU222).
(2) x8 refers to size of memory in 8-bits; x16 refers to size of memory in 16-bits.

Table 8 lists the names of the expansion bus interface signals and their functions.

Table 8. Expansion Bus Pins

PIN	DESCRIPTION
EBDMAREQ	Expansion bus DMA request
$\overline{\text{EBOE}}$	Expansion bus output enable
$\overline{\text{EBWR}}$	Expansion bus write strobe. $\overline{\text{EBWR}}$[1] controls EBDATA[15:8] and $\overline{\text{EBWR}}$[0] controls EBDATA[7:0].
$\overline{\text{EBCS}}$	Expansion bus chip select
EBADDR	Expansion bus address
EBDATA	Expansion bus data
$\overline{\text{EBHOLD}}$	Expansion bus hold: an external device connected to the expansion bus may assert this signal to add wait states to an expansion bus transaction.

MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The A384 MibADC module can function in two modes: compatibility mode, where its programmer's model is compatible with the TMS470R1x ADC module and its digital results are stored in digital result registers; or in buffered mode, where the digital result registers are replaced with three FIFO buffers, one for each conversion group [event, group1 (G1), and group2 (G2)]. In buffered mode, the MibADC buffers can be serviced by interrupts or by the DMA.

NOTE:

The MibADC on this device does not support the DMA.

MibADC Event Trigger Enhancements

The MibADC includes two major enhancements over the event-triggering capability of the TMS470R1x ADC.

- Both group1 and the event group can be configured for event-triggered operation, providing up to two event-triggered groups.
- The trigger source and polarity can be selected individually for both group1 and the event group from the options identified in Table 8.

Table 9. MibADC Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS FOR G1 OR EVENT (G1SRC[1:0] OR EVSRC[1:0])	SIGNAL PIN NAME
EVENT1	00	ADEVT
EVENT2	01	HET18
EVENT3	10	Reserved
EVENT4	11	Reserved

For group1, these event-triggered selections are configured via the group1 source select bits (G1SRC[1:0]) in the AD event source register (ADEVTSRC[5:4]). For the event group, these event-triggered selections are configured via the event group source select bits (EVSRC[1:0]) in the AD event source register (ADEVTSRC[1:0]).

For more detailed functional information on the MibADC, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

JTAG Interface

There are two main test access ports (TAPs) on the device:

- TMS470R1x CPU TAP
- Device TAP for factory test

Some of the JTAG pins are shared among these two TAPs. The hookup is illustrated in Figure 2.

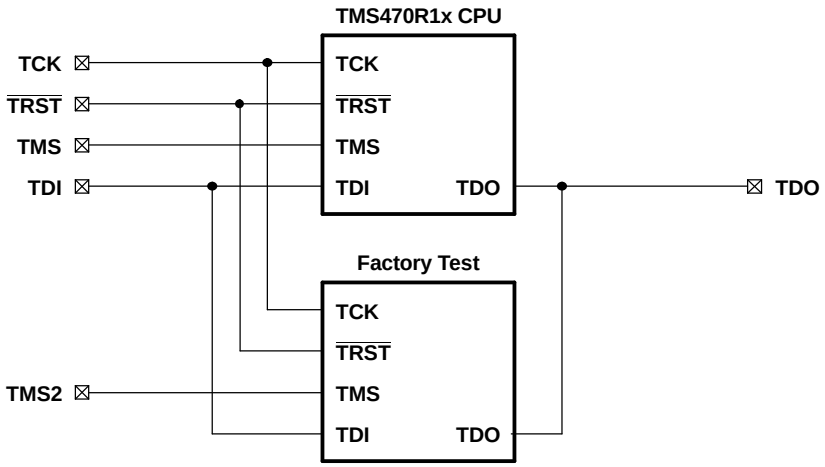


Figure 2. JTAG Interface

Documentation Support

Extensive documentation supports all of the TMS470 microcontroller family generation of devices. The types of documentation available include: data sheets with design specifications; complete user guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- Bulletin
  - *TMS470 Microcontroller Family Product Bulletin* (literature number SPNB086)
- User's Guides
  - *TMS470R1x System Module Reference Guide* (literature number SPNU189)
  - *TMS470R1x General Purpose Input/Output (GIO) Reference Guide* (literature number SPNU192)
  - *TMS470R1x Direct Memory Access (DMA) Controller Reference Guide* (literature number SPNU194)
  - *TMS470R1x Serial Peripheral Interface (SPI) Reference Guide* (literature number SPNU195)
  - *TMS470R1x Serial Communication Interface (SCI) Reference Guide* (literature number SPNU196)
  - *TMS470R1x Controller Area Network (CAN) Reference Guide* (literature number SPNU197)
  - *TMS470R1x High End Timer (HET) Reference Guide* (literature number SPNU199)
  - *TMS470R1x External Clock Prescale (ECP) Reference Guide* (literature number SPNU202)
  - *TMS470R1x MultiBuffered Analog to Digital (MibADC) Reference Guide* (literature number SPNU206)
  - *TMS470R1x Zero Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide* (literature number SPNU212)
  - *TMS470R1x F05 Flash Reference Guide* (literature number SPNU213)
  - *TMS470R1x Class II Serial Interface B (C2SIb) Reference Guide* (literature number SPNU214)
  - *TMS470R1x Class II Serial Interface A (C2SIa) Reference Guide* (literature number SPNU218)
  - *TMS470R1x JTAG Security Module (JSM) Reference Guide* (literature number SPNU245)
  - *TMS470R1x Memory Security Module (MSM) Reference Guide* (literature number SPNU246)
  - *TMS470 Peripherals Overview Reference Guide* (literature number SPNU248)
- Errata Sheet
- *TMS470R1A384 TMS470 Microcontrollers Silicon Errata* (literature number SPNZ148)

Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**470R1A384). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Figure 3 illustrates the numbering and symbol nomenclature for the TMS470R1x family.

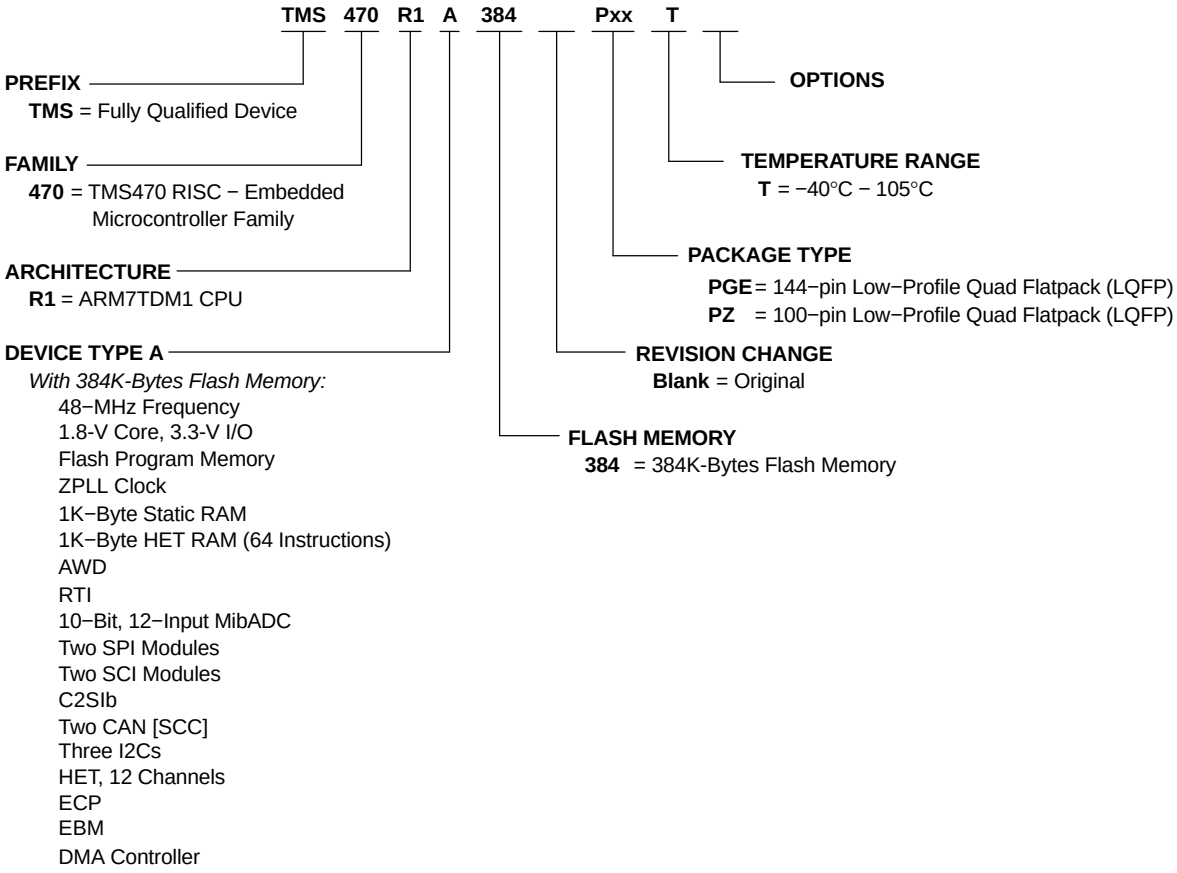


Figure 3. TMS470R1x Family Nomenclature

Device Identification Code Register

The device identification code register identifies the silicon version, the technology family (TF), a ROM or flash device, and an assigned device-specific part number (see Figure 4). The A384 device identification code register value is 0xn90F.

Figure 4. TMS470 Device ID Bit Allocation Register [offset = FFFF_FFF0h]

31	16
Reserved	

15	12	11	10	9	3	2	1	0
VERSION		TF	R/F	PART NUMBER		1	1	1
R-K		R-K	R-K	R-K		R-1	R-1	R-1

LEGEND:
R = Read only, -K = Value constant after $\overline{\text{RESET}}$; -*n* = Value after $\overline{\text{RESET}}$

Table 10. TMS470 Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31–16	Reserved		Reads are undefined and writes have no effect.
15–12	VERSION		Silicon version (revision) bits These bits identify the silicon version of the device. Initial device version numbers start at 0000.
11	TF		Technology family bit This bit distinguishes the technology family core power supply:
		0	3.3 V for F10/C10 devices
		1	1.8 V for F05/C05 devices
10	R/F		ROM/flash bit This bit distinguishes between ROM and flash devices:
		0	Flash device
		1	ROM device
9–3	PART NUMBER		Device-specific part number bits These bits identify the assigned device-specific part number. The assigned device-specific part number for the A384 device is 0100001.
2–0	1		Mandatory High Bits 2, 1, and 0 are tied high by default.

Device Electrical Specifications and Timing Parameters

Absolute Maximum Ratings

over operating free-air temperature range(1)

Supply voltage range:	V_{CC} (2)	-0.5 V to 2.5 V
Supply voltage range:	V_{CCIO} , V_{CCAD} , V_{CCP} (flash pump) (2)	-0.5 V to 4.1V
Input voltage range:	All 5 V- tolerant input pins	-0.5 V to 6.0V
	All other input pins	-0.5 V to 4.1V
Input clamp current:	All 5-V tolerant pins, $\overline{PORRST}$, $\overline{TRST}$, TEST, and TCK (V_I < 0)	-20 mA (3)
	ADIN[0:11] I_{IK} (V_I < 0 or V_I > V_{CCAD})	±10 mA
	All other pins I_{IK} (V_I < 0 or V_I > V_{CCAD})	±20 mA
Operating free-air temperature ranges, T_A	T version	-40°C to 105°C
Operating junction temperature range, T_J		-40°C to 150°C
Storage temperature range, T_{stg}		-40°C to 150°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.
(3) These pins do not have an internal clamp diode to a positive supply voltage.

Device Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)		1.71		2.05	V
V_{CCIO}	Digital logic supply voltage (I/O)		3	3.3	3.6	V
V_{CCAD}	MibADC supply voltage		3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	MibADC supply ground		-0.1		0.1	V
T_A	Operating free-air temperature	T version	-40		105	° C
T_J	Operating junction temperature		-40		150	° C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

Electrical Characteristics

over recommended operating free-air temperature range(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			0.15			V
V_{IL}	Low-level input voltage	All inputs(2) except OSCIN		-0.3		0.8	V
		OSCIN only		-0.3		0.35 V_{CC}	
V_{IH}	High-level input voltage	All inputs except OSCIN		2		V_{CCIO} + 0.3	V
		OSCIN only		0.65 VCC		V_{CC} + 0.3	
V_{th}	Input threshold voltage	AWD only		1.35		1.8	V
RDS_{ON}	Drain to source on resistance	AWD only (3)	V_{OL} - 0.35 V @ I_{OL} = 4 mA			90	
V_{OL}	Low-level output voltage(4)		I_{OL} = I_{OL} MAX			0.2 V_{CCIO}	V
			I_{OL} = 3 mA			0.4	
V_{OH}	High-level output voltage(4)		I_{OH} = I_{OH} MIN	0.8 V_{CCIO}			V
			I_{OH} = 250 µA	2.7			
I_{IC}	Input clamp current (I/O pins)(5)		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIO} + 0.3	-2		2	mA
I_I	Input current (3.3 V input pins)	I_{IL} Pulldown	V_I = V_{SS}	-1		1	µA
		I_{IH} Pulldown	V_I = V_{CCIO}	5		40	
		I_{IL} Pullup	V_I = V_{SS}	-40		-5	
		I_{IH} Pullup	V_I = V_{CCIO}	-1		1	
		All other pins	No pullup or pulldown	-1		1	
	Input current (5 V tolerant input pins)		V_I = V_{SS}	-1		1	µA
			V_I = V_{CCIO}	-1		1	
			V_I = 5 V	0.5		20	
			V_I = 5.5 V	1		40	
I_{OL}	Low-level output current	$\overline{RST}$, CLKOUT, AWD, TDO	V_{OL} = V_{OL} MAX			4	mA
		All other 3.3 V I/O(6)				2	
		5-V tolerant				4	
I_{OH}	High-level output current	$\overline{RST}$, CLKOUT, TDO	V_{OH} = V_{OH} MIN	-4			mA
		All other 3.3 V I/O(6)		-2			
		5 V tolerant		-4			
I_{CC}	V_{CC} Digital supply current (operating mode)		SYSCLK = 24 MHz, ICLK = 15 MHz, V_{CC} = 2.05 V			90	mA
			SYSCLK = 48 MHz, ICLK = 24MHz, V_{CC} = 2.05 V			115	
	V_{CC} Digital supply current (standby mode)(7)		OSCIN = 4 MHz, V_{CC} = 2.05 V			1.25	µA
	V_{CC} Digital supply current (halt mode)(7)		30°C version, V_{CC} = 2.05 V			30	µA
			T version (105°C), V_{CC} = 2.05 V			550	

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the *$\overline{RST}$ and $\overline{PORRST}$ Timings* section.
(3) These values help to determine the external RC network circuit. For more details, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).
(4) V_{OL} and V_{OH} are linear with respect to the amount of load current (I_{OL}/I_{OH}) applied.
(5) Parameter does not apply to input-only or output-only pins.
(6) The 2 mA buffers on this device are called zero-dominant buffers. If two of these buffers are shorted together and one is outputting a low level and the other is outputting a high level, the resulting value will always be low.
(7) For flash banks/pumps in sleep mode.

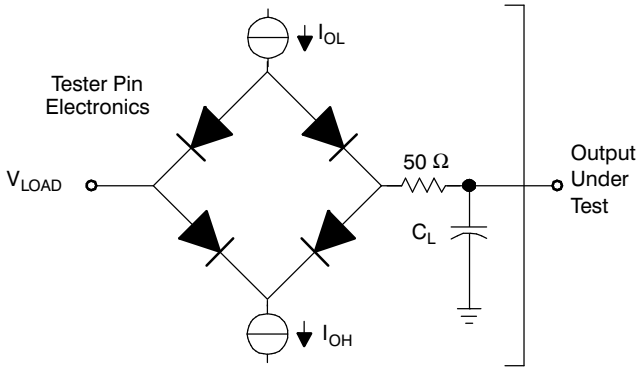
Electrical Characteristics (continued)

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)	No DC load, V_{CCIO} = 3.6 V(8)			10	mA
	V_{CCIO} Digital supply current (standby mode)	No DC load, V_{CCIO} = 3.6 V(8)			15	µA
	V_{CCIO} Digital supply current (halt mode)	No DC load, V_{CCIO} = 3.6 V(8)			5	µA
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V			25	mA
	V_{CCAD} supply current (standby mode)	No DC load, V_{CCAD} = 3.6 V(8)			10	µA
	V_{CCAD} supply current (halt mode)	V_{CCAD} = 3.6 V			5	µA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation			25	mA
		V_{CCP} = 3.6 V program and erase			70	mA
		V_{CCP} = 3.6 V standby mode operation(7)			10	µA
		V_{CCP} = 3.6 V halt mode operation(7)			5	µA
C_I	Input capacitance			2		pF
C_O	Output capacitance			3		pF

(8) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V.

Parameter Measurement Information



Where: I_{OL} = I_{OL} MAX for the respective pin (A)
I_{OH} = I_{OH} MIN for the respective pin(A)
V_{LOAD} = 1.5 V
C_L = 150-pF typical load-circuit capacitance(B)

A. For these values, see the "Electrical Characteristics over Recommended Operating Free-Air Temperature Range" table.

B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

Figure 5. Test Load Circuit

Timing Parameter Symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

CM	Compaction, CMPCT	RD	Read
CO	CLKOUT	RST	Reset, $\overline{\text{RST}}$
ER	Erase	RX	SCInRX
ICLK	Interface clock	S	Slave mode
M	Master mode	SCC	SCInCLK
OSC, OSCI	OSCIN	SIMO	SPInSIMO
OSCO	OSCOUT	SOMI	SPInSOMI
P	Program, PROG	SPC	SPInCLK
R	Ready	SYS	System clock
R0	Read margin 0, RDMRGN0	TX	SCInTX
R1	Read margin 1, RDMRGN1		

Lowercase subscripts and their meanings are:

a	access time	r	rise time
c	cycle time (period)	su	setup time
d	delay time	t	transition time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

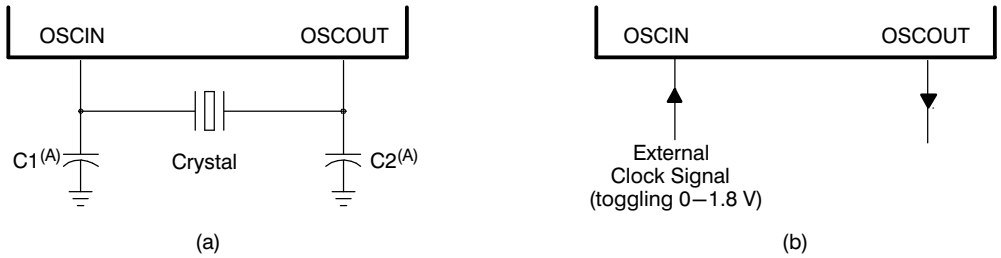
The following additional letters are used with these meanings:

H	High	X	Unknown, changing, or don't care level
L	Low	Z	High impedance
V	Valid		

External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 4-20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 6a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 6b.



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 6. Crystal/Clock Connection

ZPLL AND CLOCK SPECIFICATIONS

Timing Requirements for ZPLL Circuits Enabled or Disabled

		MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	4		20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50			ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15			ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15			ns
$f_{(OSCRST)}$	OSC FAIL frequency (1)		53		kHz

(1) Causes a device reset (specifically a clock reset) by setting the RST OSC FAIL (GLBCTRL.15) and the OSC FAIL flag (GLBSTAT.1) bits equal to 1. For more detailed information on these bits and device resets, see the *TMS470R1x System Module Reference Guide* (literature number SPNU189).

Switching Characteristics Over Recommended Operating Conditions for Clocks (1) (2)

PARAMETER		TEST CONDITIONS (3)	MIN	MAX	UNIT
$f_{(SYS)}$	System clock frequency (4)	Pipeline mode enabled		48	MHz
		Pipeline mode disabled		24	MHz
$f_{(CONFIG)}$	System clock frequency - flash config mode			24	MHz
$f_{(ICLK)}$	Interface clock frequency			24	MHz
$f_{(ECLK)}$	External clock output frequency for ECP module			24	MHz
$t_{c(SYS)}$	Cycle time, system clock	Pipeline mode enabled	20.8		ns
		Pipeline mode disabled	41.6		ns
$t_{c(CONFIG)}$	Cycle time, system clock - flash config mode		41.6		ns
$t_{c(ICLK)}$	Cycle time, interface clock		41.6		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output		41.6		ns

(1) $f_{(SYS)} = M \times f_{(OSC)} / R$, where M = {8}, R = {1,2,3,4,5,6,7,8} when PLLDIS = 0. R is the system-clock divider determined by the CLKDIVPRE [2:0] bits in the global control register (GLBCTRL[2:0]) and M is the PLL multiplier determined by the MULT4 bit also in the GLBCTRL register (GLBCTRL.3).
$f_{(SYS)} = f_{(OSC)} / R$, where R = {1,2,3,4,5,6,7,8} when PLLDIS = 1.
$f_{(ICLK)} = f_{(SYS)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) $f_{(ECLK)} = f_{(ICLK)} / N$, where N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).
(4) Flash Vread must be set to 5 V to achieve maximum system clock frequency.

Switching Characteristics Over Recommended Operating Conditions for External Clocks(1)(2)(3)

(see Figure 7 and Figure 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(COL)}$	Pulse duration, CLKOUT low	SYSCLK or MCLK(4)	$0.5t_{c(SYS)} - t_f$		ns
		ICLK: X is even or 1(5)	$0.5t_{c(ICLK)} - t_f$		
		ICLK: X is odd and not 1(5)	$0.5t_{c(ICLK)} + 0.5t_{c(SYS)} - t_f$		
$t_{w(COH)}$	Pulse duration, CLKOUT high	SYSCLK or MCLK(4)	$0.5t_{c(SYS)} - t_r$		ns
		ICLK: X is even or 1(5)	$0.5t_{c(ICLK)} - t_r$		
		ICLK: X is odd and not 1(5)	$0.5t_{c(ICLK)} - 0.5t_{c(SYS)} - t_r$		
$t_{w(EOL)}$	Pulse duration, ECLK low	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_f$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} - t_f$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} + 0.5t_{c(SYS)} - t_f$		
$t_{w(EOH)}$	Pulse duration, ECLK high	N is even and X is even or odd	$0.5t_{c(ECLK)} - t_r$		ns
		N is odd and X is even	$0.5t_{c(ECLK)} - t_r$		
		N is odd and X is odd and not 1	$0.5t_{c(ECLK)} - 0.5t_{c(SYS)} - t_r$		

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the interface clock divider ratio determined by the PCR0[4:1] bits in the SYS module.
(2) N = {1 to 256}. N is the ECP prescale value defined by the ECPCTRL[7:0] register bits in the ECP module.
(3) CLKOUT/ECLK pulse durations (low/high) are a function of the OSCIN pulse durations when PLLDIS is active.
(4) Clock source bits are selected as either SYSCLK (CLKCNTL[6:5] = 11 binary) or MCLK (CLKCNTL[6:5] = 10 binary).
(5) Clock source bits are selected as ICLK (CLKCNTL[6:5] = 01 binary).

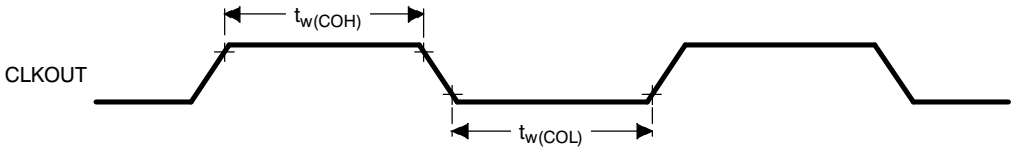


Figure 7. CLKOUT Timing Diagram

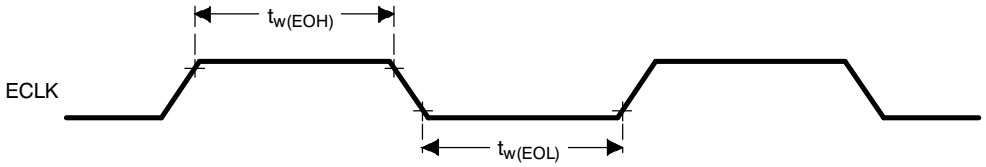


Figure 8. ECLK Timing Diagram

$\overline{\text{RST}}$ AND $\overline{\text{PORRST}}$ TIMINGS

Timing Requirements for $\overline{\text{PORRST}}$

(see Figure 9)

		MIN	MAX	UNIT
V_{CCPORL}	V_{CC} low supply level when $\overline{\text{PORRST}}$ must be active during power up		0.6	V
V_{CCPORH}	V_{CC} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	1.5		V
$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	2.75		V
V_{IL}	Low-level input voltage after $V_{CCIO} > V_{CCIOPORH}$		0.2 V_{CCIO}	V
$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before V CCIO > $V_{CCIOPORL}$		0.5	V
$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIO} > V_{CCIOPORL}$ during power up	0		ms
$t_{su(VCCIO)r}$	Setup time, $V_{CCIO} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCPORH}$ during power down	8		µs
$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCIOPORH}$	1		ms
$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} < V_{CCPORL}$	0		ms
$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \leq V_{CCIOPORH}$ during power down	0		ns
$t_{su(VCCIO)f}$	Setup time, $V_{CC} < V_{CCPORL}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns

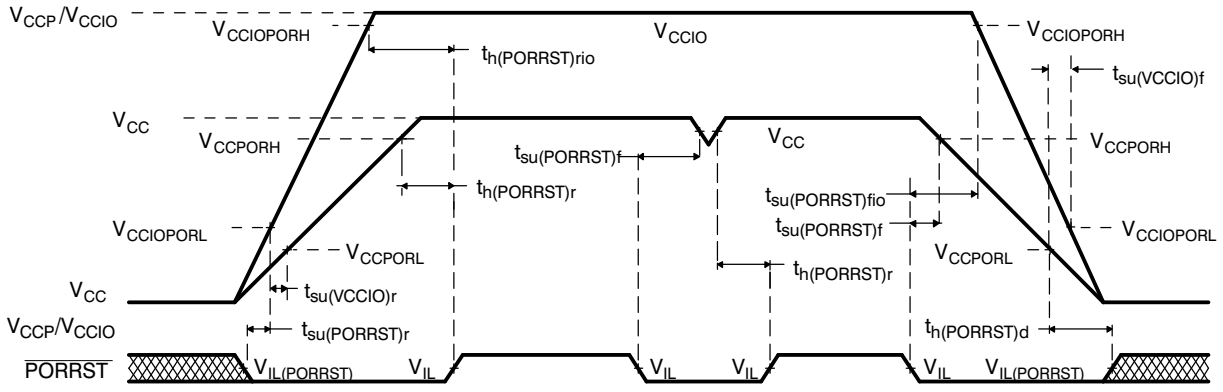


Figure 9. $\overline{\text{PORRST}}$ Timing Diagram

Switching Characteristics Over Recommended Operating Conditions for $\overline{\text{RST}}$(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$4112t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(SYS)}$		
t_{fsu}	Flash start-up time, from $\overline{\text{RST}}$ inactive to fetch of first instruction from flash (flash pump stabilization time)	$360t_{c(OSC)}$		ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.

JTAG SCAN INTERFACE TIMING

(JTAG Clock Specification 10-MHz and 50-pF Load on TDO Output)

		MIN	MAX	UNIT
$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	15		ns
$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	15		ns
$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	10		ns
$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

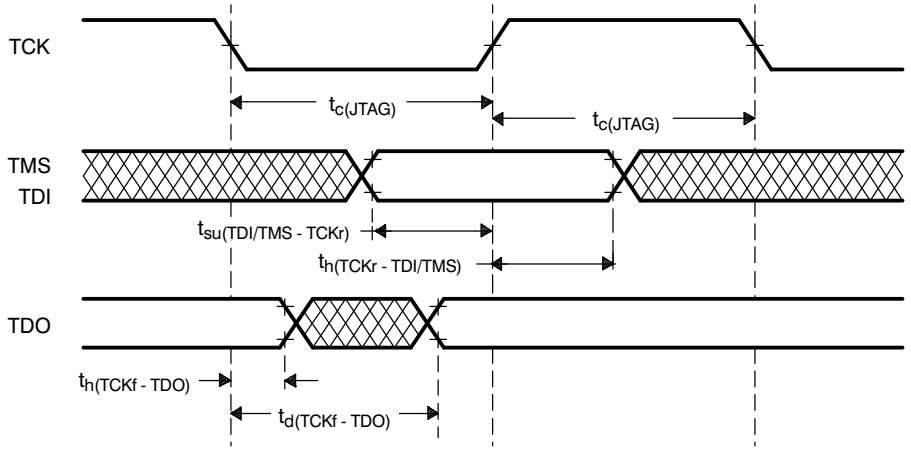


Figure 10. JTAG Scan Timings

OUTPUT TIMINGS

Switching Characteristics for Output Timings versus Load Capacitance (C_L)

(see Figure 11)

PARAMETER			MIN	MAX	UNIT
t_r	Rise time, AWD, CLKOUT, $\overline{RST}$, TD0/GIOC[6]	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_f	Fall time, AWD, CLKOUT, TDO/GIOC[6]	C_L = 15 pF	2.5	8	ns
		C_L = 50 pF	5	14	
		C_L = 100 pF	9	23	
		C_L = 150 pF	13	32	
t_r	Rise time, 4mA, 5 V tolerant pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	3.5	12	
		C_L = 100 pF	7	21	
		C_L = 150 pF	9	28	
t_f	Fall time,4mA, 5 V tolerant pins	C_L = 15 pF	2	8	ns
		C_L = 50 pF	2.5	9	
		C_L = 100 pF	8	25	
		C_L = 150 pF	11	35	
t_r	Rise time, all other output pins	C_L = 15 pF	2.5	10	ns
		C_L = 50 pF	6.0	25	
		C_L = 100 pF	12	45	
		C_L = 150 pF	18	65	
t_f	Fall time, all other output pins	C_L = 15 pF	3	10	ns
		C_L = 50 pF	8.5	25	
		C_L = 100 pF	16	45	
		C_L = 150 pF	23	65	

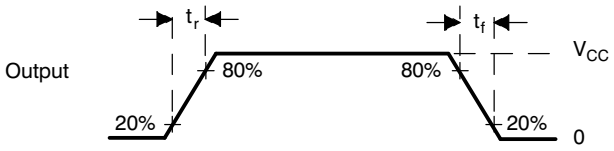


Figure 11. CMOS-Level Outputs

INPUT TIMINGS

Timing Requirements for Input Timings[1]

(see Figure 12)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(ICLK)}$ + 10		ns

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$

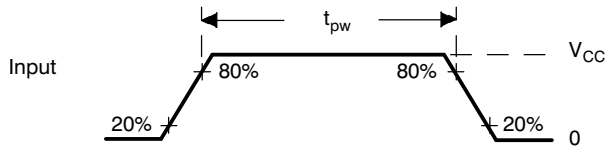


Figure 12. CMOS-Level Inputs

FLASH TIMINGS

Timing Requirements for Program Flash[1]

		MIN	TYP	MAX	UNIT
$t_{prog(16\text{-}bit)}$	Half word (16-bit) programming time	4	16	200	µs
$t_{prog(Total)}$	384K-byte programming time[2]		3	10	s
$t_{erase(sector)}$	Sector erase time		2	15	s
t_{wec}	Write/erase cycles at T_A = 105°C	1000	10000		cycles
$t_{fp(RST)}$	Flash pump settling time from $\overline{RST}$ to SLEEP		$72t_{c(SYS)}$		ns
$t_{fp(SLEEP)}$	Initial flash pump settling time from SLEEP to STANDBY		$72t_{c(SYS)}$		
$t_{fp(STANDBY)}$	Initial flash pump settling time from STANDBY to ACTIVE		$36t_{c(SYS)}$		

(1) For more detailed information on the flash core sectors, see the *flash program and erase* section of this data sheet.
(2) The 384K-byte programming time includes overhead of state machine.

SPIn MASTER MODE TIMING PARAMETERS

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 13)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0)		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1)		10	
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	$t_{c(SPC)M} - 5 - t_f$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	$t_{c(SPC)M} - 5 - t_r$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 1)	6		
7(5)	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0)	4		ns
	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

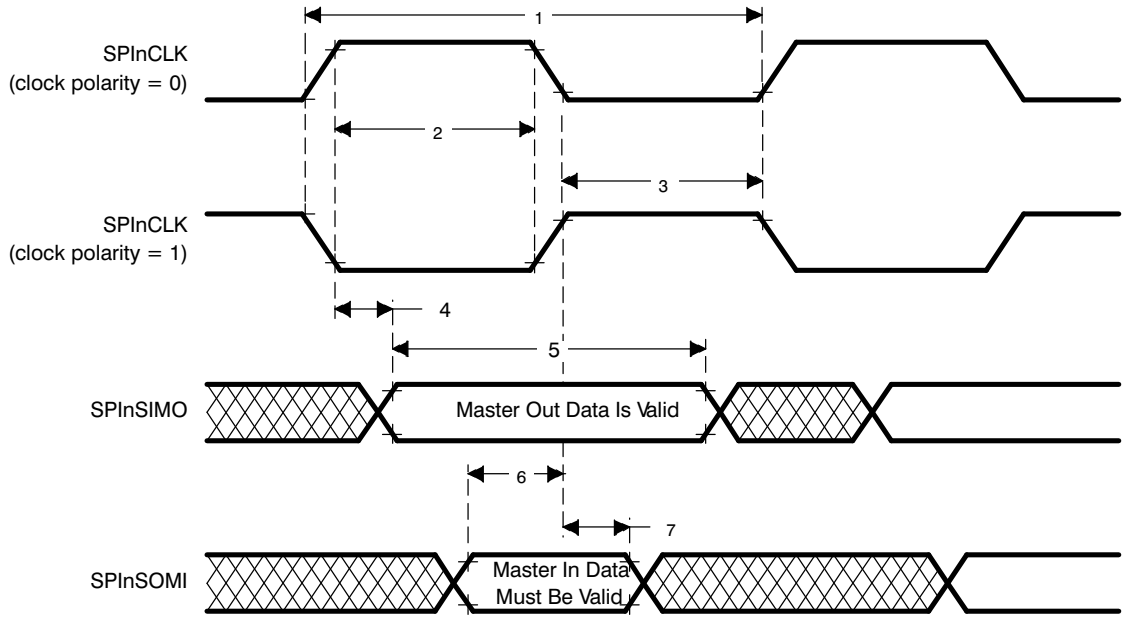


Figure 13. SPIn Master Mode External Timing (CLOCK PHASE = 0)

SPIn Master Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 14)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPInCLK(4)	100	$256t_{c(ICLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - 10$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - 10$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 5 - t_r$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 5 - t_f$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPInSOMI before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPInSOMI before SPInCLK low (clock polarity = 1)	6		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	4		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	4		

(1) The MASTER bit (SPInCTRL2.3) is set and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) When the SPI is in master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(ICLK)} \geq 100$ ns.
(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

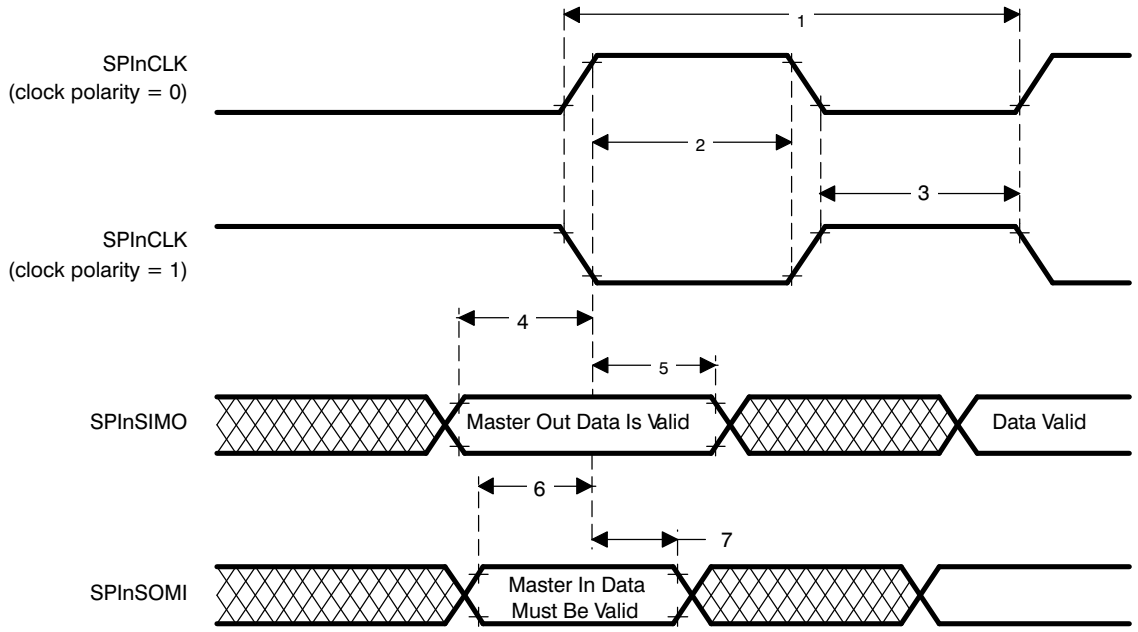


Figure 14. SPIn Master Mode External Timing (CLOCK PHASE = 1)

SPIn SLAVE MODE TIMING PARAMETERS

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 15)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$6 + t_r$	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$6 + t_f$	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$t_{c(SPC)S} - 6 - t_f$		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	6		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

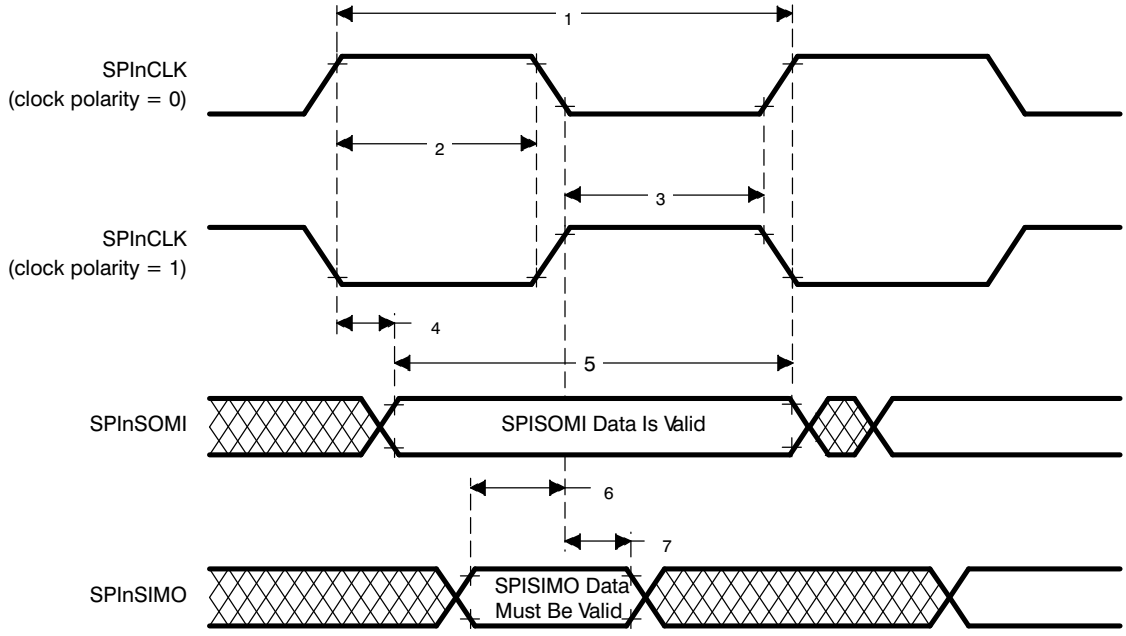


Figure 15. SPIn Slave Mode External Timing (CLOCK PHASE = 0)

SPIn Slave Mode External Timing Parameters

(CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4) (see Figure 16)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	100	$256t_{c(ICLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	$0.5t_{c(SPC)S} - 0.25t_{c(ICLK)}$	$0.5t_{c(SPC)S} + 0.25t_{c(ICLK)}$	
4(6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	$0.5t_{c(SPC)S} - 6 - t_r$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	$0.5t_{c(SPC)S} - 6 - t_f$		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	6		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	6		
7(6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(ICLK)}$, where PS = prescale value set in SPInCTL1[12:5].
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(4) $t_{c(ICLK)}$ = interface clock cycle time = $1 / f_{(ICLK)}$
(5) When the SPIn is in slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(ICLK)} \geq 100$ ns, where PS is the prescale value set in the SPInCTL1[12:5] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(ICLK)} \geq 100$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPInCTRL2[1]).

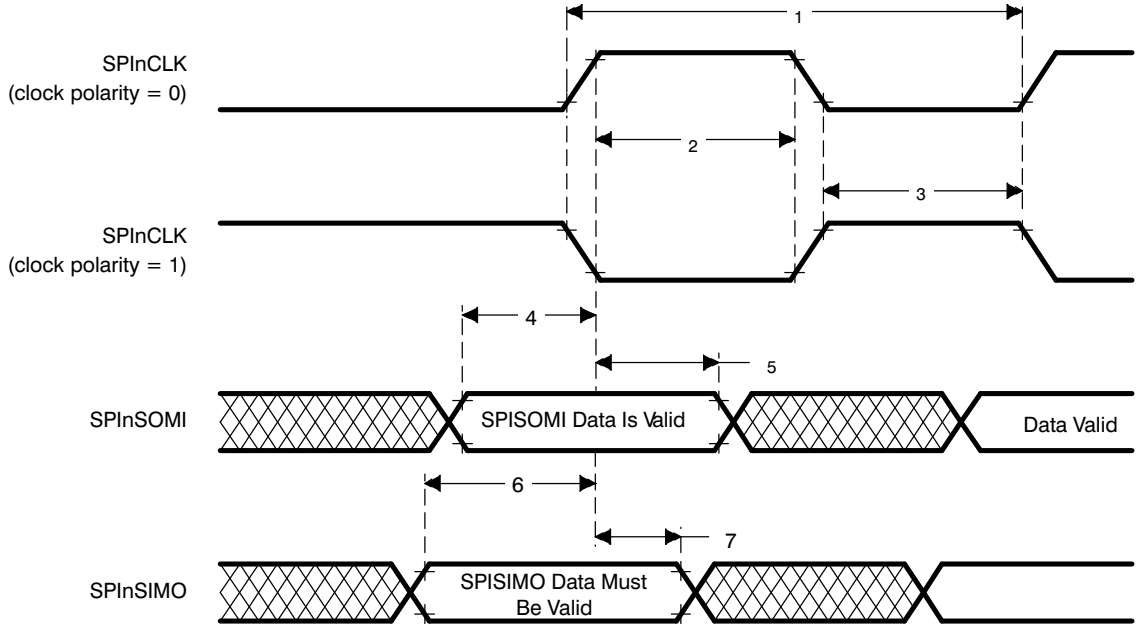


Figure 16. SPIn Slave Mode External Timing (CLOCK PHASE = 1)

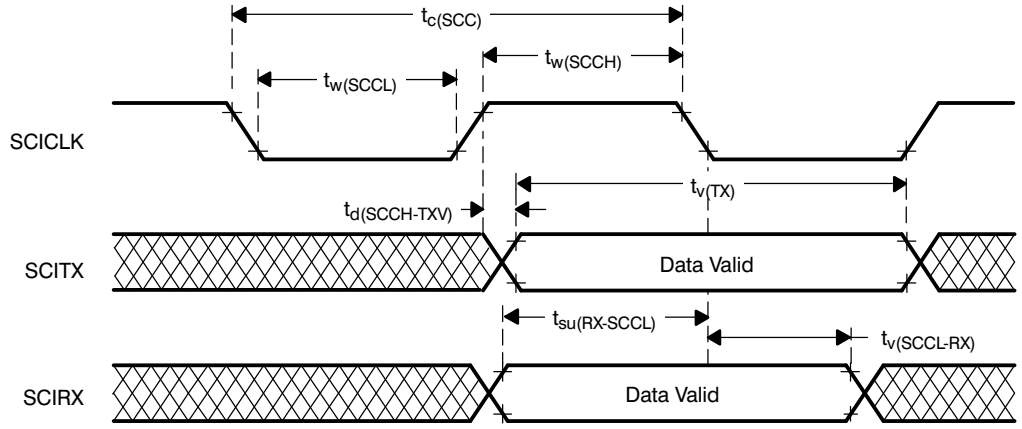
SCIn ISOSYNCHRONOUS MODE TIMINGS INTERNAL CLOCK

Timing Requirements for Internal Clock SCIn Isosynchronous Mode(1)(2)(3)

(see Figure 17)

		(BAUD + 1) IS EVEN OR BAUD = 0		(BAUD + 1) IS ODD AND BAUD ≠ 0		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCC)}$	Cycle time, SCInCLK	$2t_{c(ICLK)}$	$2^{24}\ t_{c(ICLK)}$	$3t_{c(ICLK)}$	$(2^{24}-1)\ t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - t_f$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)} - t_f$	$0.5t_{c(SCC)} + 0.5t_{c(ICLK)}$	ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - t_r$	$0.5t_{c(SCC)} + 5$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)} - t_r$	$0.5t_{c(SCC)} - 0.5t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		10		10	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$t_{c(SCC)} - 10$		$t_{c(SCC)} - 10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	$t_{c(ICLK)} + t_f + 20$		$t_{c(ICLK)} + t_f + 20$		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$-t_{c(ICLK)} + t_f + 20$		$- t_{c(ICLK)} + t_f + 20$		ns

(1) BAUD = 24-bit concatenated value formed by the SCI[H,M,L]BAUD registers.
(2) $t_{c(ICLK)}$ = interface clock cycle time = $1/f_{(ICLK)}$
(3) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.



A. Data transmission/reception characteristics for isosynchronous mode with internal clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 17. SCIn Isosynchronous Mode Timing Diagram for Internal Clock

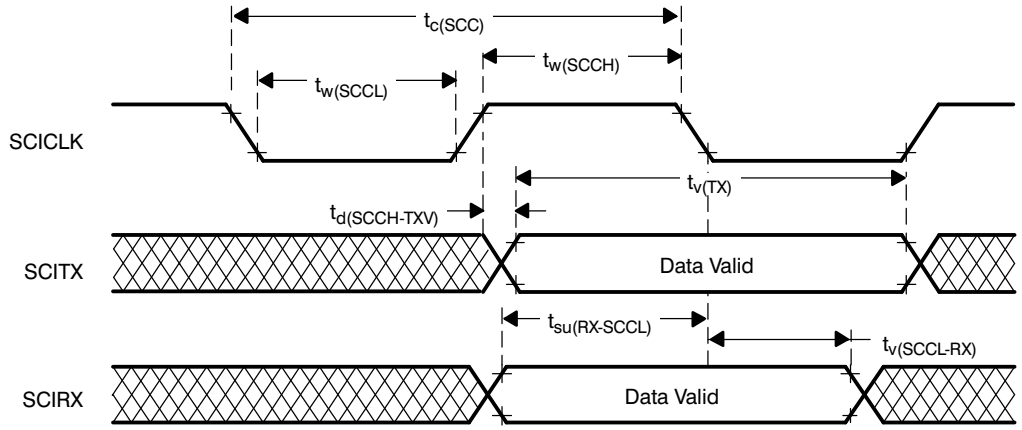
SCIn ISOSYNCHRONOUS MODE TIMINGS EXTERNAL CLOCK

Timing Requirements for External Clock SCIn Isosynchronous Mode(1)(2)

(see Figure 18)

		MIN	MAX	UNIT
$t_{c(SCC)}$	Cycle time, SCInCLK(3)	$8t_{c(ICLK)}$		ns
$t_{w(SCCH)}$	Pulse duration, SCInCLK high	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{w(SCCL)}$	Pulse duration, SCInCLK low	$0.5t_{c(SCC)} - 0.25t_{c(ICLK)}$	$0.5t_{c(SCC)} + 0.25t_{c(ICLK)}$	ns
$t_{d(SCCH-TXV)}$	Delay time, SCInCLK high to SCInTX valid		$2t_{c(ICLK)} + 12 + t_r$	ns
$t_{v(TX)}$	Valid time, SCInTX data after SCInCLK low	$2t_{c(SCC)} -10$		ns
$t_{su(RX-SCCL)}$	Setup time, SCInRX before SCInCLK low	0		ns
$t_{v(SCCL-RX)}$	Valid time, SCInRX data after SCInCLK low	$2t_{c(ICLK)} + 10$		ns

(1) $t_{c(ICLK)}$ = interface clock cycle time = 1 / $f_{(ICLK)}$
(2) For rise and fall timings, see the "Switching Characteristics for Output Timings versus Load Capacitance" table.
(3) When driving an external SCInCLK, the following must be true: $t_{c(SCC)} \geq 8t_{c(ICLK)}$.



A. Data transmission / reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception occurs on the SCICLK falling edge.

Figure 18. SCIn Isosynchronous Mode Timing Diagram for External Clock

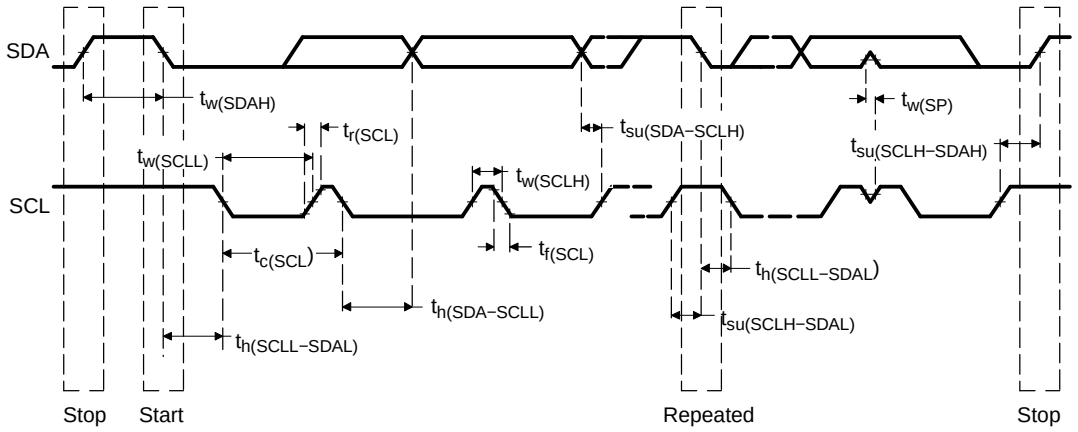
I2C TIMING

Table 11 below assumes testing over recommended operating conditions.

Table 11. I2C Signals (SDA and SCL) Switching Characteristics(1)

PARAMETER			STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(I2CCLK)}$	Cycle time, I2C module clock		75	150	75	150	ns
$t_{c(SCL)}$	Cycle time, SCL		10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)		4.7		0.6		µ s
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a repeated START condition)		4		0.6		µ s
$t_{w(SCLL)}$	Pulse duration, SCL low		4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high		4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high		250		100		ns
$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	For I2C bus devices	0	3.45(2)	0	0.9	µ s
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions		4.7		1.3		µ s
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)		4.0		0.6		µ s
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)				0	50	ns
C_b(3)	Capacitive load for each bus line			400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices needs only be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) C_b = The total capacitance of one bus line in pF.



A. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

B. The maximum $t_{h(SDA-SCLL)}$ needs only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.

C. A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$.

D. C_b = total capacitance of one bus line in pF. If mixed with HS=mode devices, faster fall-times are allowed.

Figure 19. I2C Timings

STANDARD CAN CONTROLLER (SCC) MODE TIMINGS

Dynamic Characteristics for the CANSTX and CANSRX Pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANSTX)}$	Delay time, transmit shift register to CANSTX pin (1)		15	ns
$t_{d(CANSRX)}$	Delay time, CANSRX pin to receive shift register		5	ns

(1) These values do not include the rise/fall times of the output buffer.

EXPANSION BUS MODULE TIMING

Expansion Bus Timing Parameters, -40°C ≤ T_J ≤ 150°C, 3.0 V ≤ V_{CC} ≤ 3.6 V

(see Figure 20 and Figure 21)

		MIN	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	20.8		ns
$t_{d(COH-EBADV)}$	Delay time, CLKOUT high to EBADDR valid		21.4	ns
$t_{h(COH-EBADIV)}$	Hold time, EBADDR invalid after CLKOUT high		12.4	ns
$t_{d(COH-EBOE)}$	Delay time, CLKOUT high to $\overline{EBOE}$ fall		11.4	ns
$t_{h(COH-EBOEH)}$	Hold time, $\overline{EBOE}$ rise after CLKOUT high		11.4	ns
$t_{d(COL-EBWR)}$	Delay time, CLKOUT low to write strobe ($\overline{EBWR}$) low		11.3	ns
$t_{h(COL-EBWRH)}$	Hold time, $\overline{EBWR}$ high after CLKOUT low		11.6	ns
$t_{su(EBRDATV-COH)}$	Setup time, EBDATA valid before CLKOUT high (READ) (1)	15.2		ns
$t_{h(COH-EBRDATIV)}$	Hold time, EBDATA invalid after CLKOUT high (READ)		(-14.7)	ns
$t_{d(COL-EBWDATV)}$	Delay time, CLKOUT low to EBDATA valid (WRITE) (2)		16.1	ns
$t_{h(COL-EBWDATIV)}$	Hold time, EBDATA invalid after CLKOUT low (WRITE)		14.7	ns
SECONDARY TIMES				
$t_{d(COH-EBCS0)}$	Delay, CLKOUT high to $\overline{EBCS0}$ fall		13.6	ns
$t_{h(COH-EBCS0H)}$	Hold, $\overline{EBCS0}$ rise after CLKOUT high		13.2	ns
$t_{su(COH-EBHOLDL)}$	Setup time, $\overline{EBHOLD}$ low to CLKOUT high (1)	10.9		ns
$t_{su(COH-EBHOLDH)}$	Setup time, $\overline{EBHOLD}$ high to CLKOUT high (1)	10.5		ns

(1) Setup time is the minimum time under worst case conditions. Data with less setup time will not work.
(2) Valid after CLKOUT goes low for write cycles.

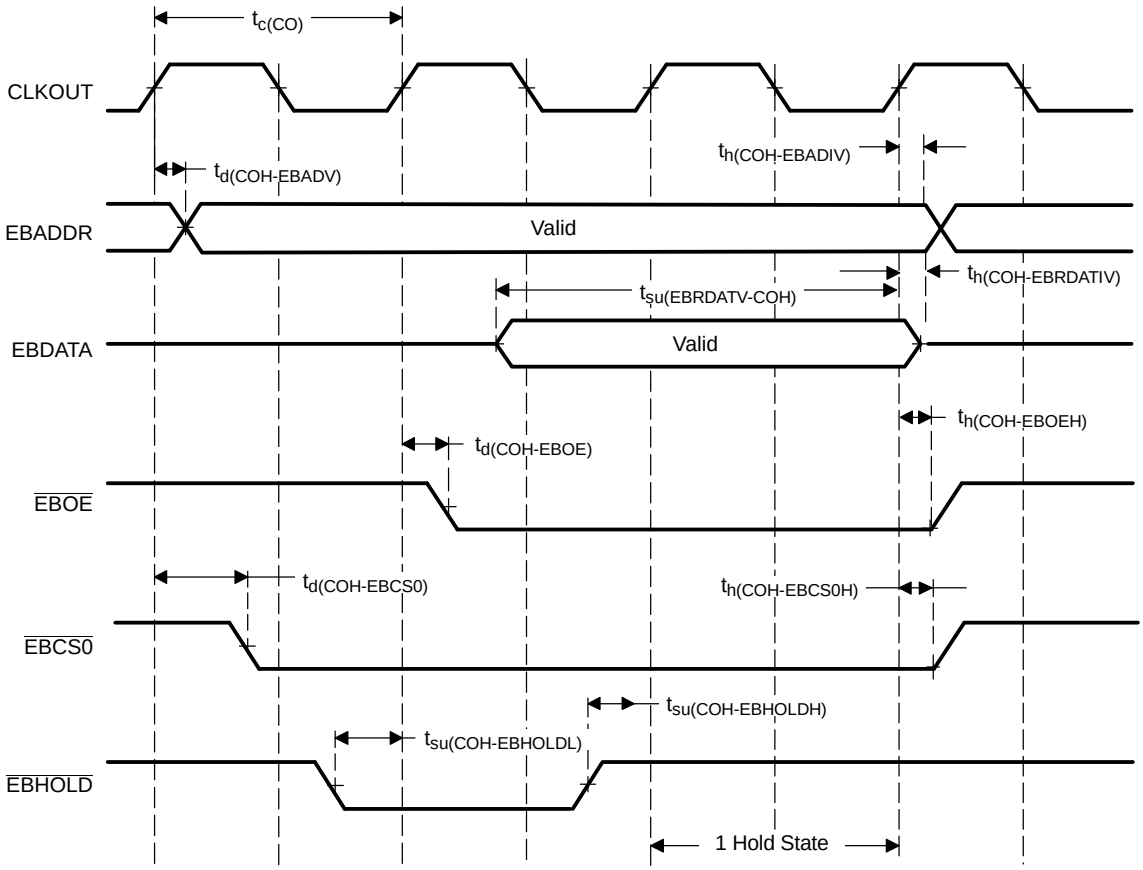


Figure 20. Expansion Memory Signal Timing - Reads

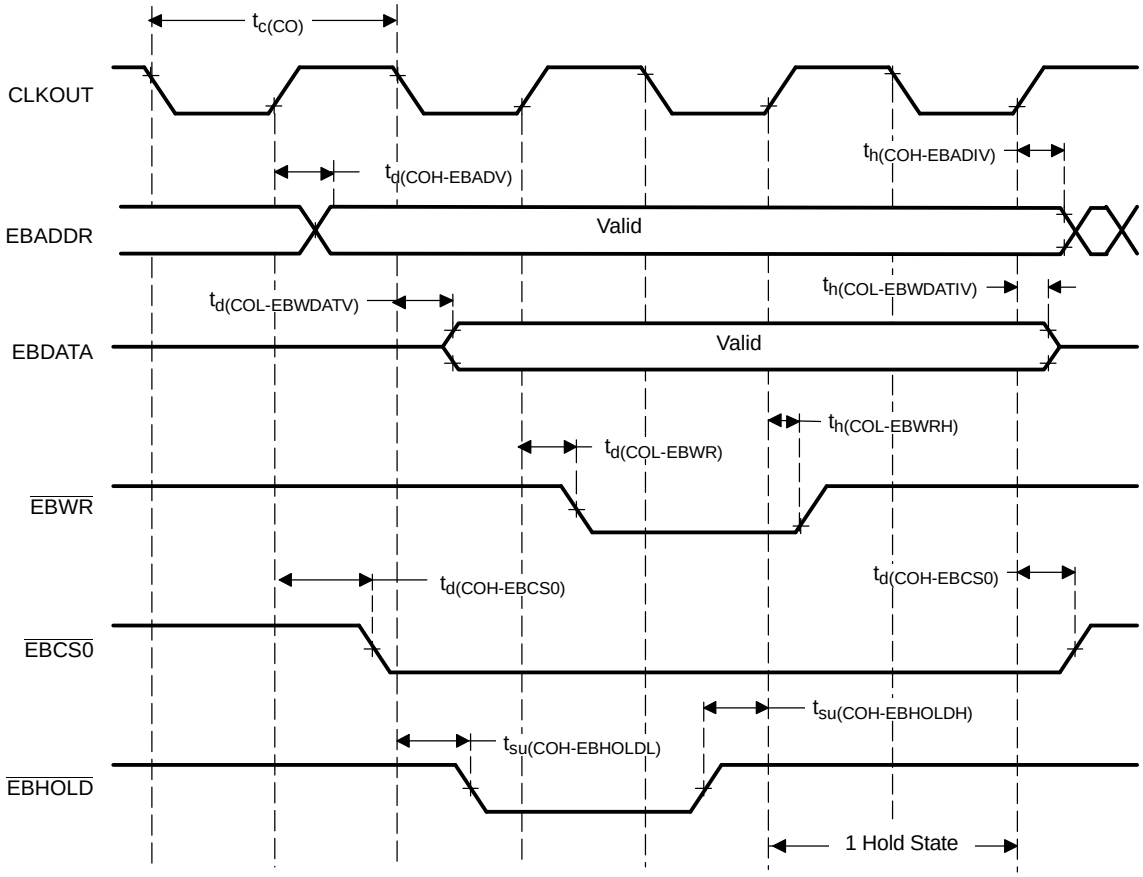


Figure 21. Expansion Memory Signal Timing - Writes

CLASS 2 SERIAL INTERFACE B (C2SIb) VARIABLE PULSE WIDTH (VPW) MODULATION

VPW Timing Requirements

See Figure 22.

PARAMETER		NORMAL MODE (10.4 KBPS)				4X MODE (41.6 KBPS)				UNIT
		TX		RX		TX		RX		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
SOF	Start of frame	192	208	163	239	48	52	41	60	ns
Short Pulse	Low = 0	60	68	34	96	14	18	9	24	ns
	High = 1									
Long Pulse	Low = 0	122	134	97	163	30	34	24	41	ns
	High = 1									
EOD	End of data	193	207	164	239	48	52	41	60	ns
NB	Normalization bit (long)	122	134	97	163	30	34	24	41	ns
	Normalization bit (short)	60	68	34	96	14	18	9	24	
EOF	End of frame	271	289	240	320	67	73	60	80	ns
Break	Short	290	-	239	-	290	-	60	-	ns
	Long	758	-	239	-	758	-	60	-	

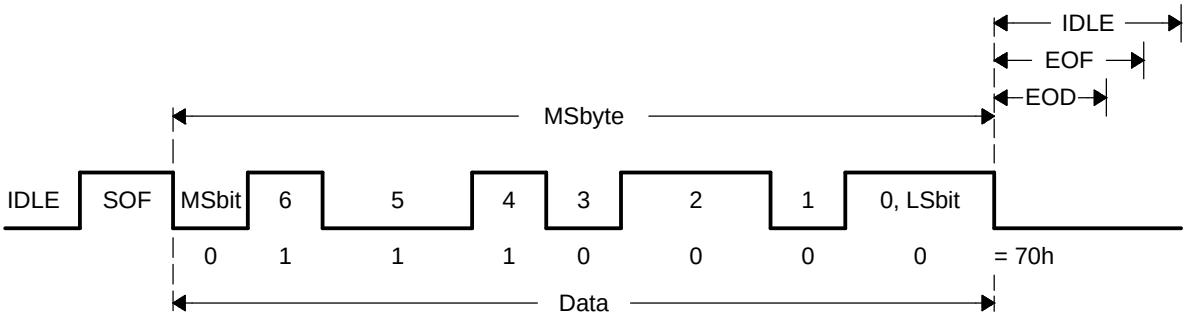


Figure 22. C2SIb Timing Diagram

HIGH-END TIMER (HET) TIMINGS

Minimum PWM Output Pulse Width:

This is equal to one high resolution clock period (HRP). The HRP is defined by the 6-bit high resolution prescale factor (hr), which is user defined, giving prescale factors of 1 to 64, with a linear increment of codes.

Therefore, the minimum PWM output pulse width = HRP(min) = hr(min)/SYSCLK = 1/SYSCLK

For example, for a SYSCLK of 30 MHz, the minimum PWM output pulse width = 1/30 = 33.33ns

Minimum Input Pulses that Can Be Captured:

The input pulse width must be greater or equal to the low resolution clock period (LRP), i.e., the HET loop (the HET program must fit within the LRP). The LRP is defined by the 3-bit loop-resolution prescale factor (lr), which is user defined, with a power of 2 increment of codes. That is, the value of lr can be 1, 2, 4, 8, 16, or 32.

Therefore, the minimum input pulse width = LRP(min) = hr(min) * lr(min)/SYSCLK = 1 * 1/SYSCLK

For example, with a SYSCLK of 30 MHz, the minimum input pulse width = 1 * 1/30 = 33.33 ns

NOTE:

Once the input pulse width is greater than LRP, the resolution of the measurement is still HRP. (That is, the captured value gives the number of HRP clocks inside the pulse.)

Abbreviations:

hr = HET high resolution divide rate = 1, 2, 3,...63, 64

lr = HET low resolution divide rate = 1, 2, 4, 8, 16, 32

High resolution clock period = HRP = hr/SYSCLK

Loop resolution clock period = LRP = hr*lr/SYSCLK

MULTI-BUFFERED A-TO-D CONVERTER (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry, which could be present on V_{SS} and V_{CC}, from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

Table 12. MibADC Recommended Operating Conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	V_{SSAD}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	V_{CCAD}	V
V_{AI}	Analog input voltage	V_{SSAD} - 0.3	V_{CCAD} + 0.3	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD}$ - 0.3 or $V_{AI} > V_{CCAD}$ + 0.3)	-2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see the "Device Recommended Operating Conditions" table.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 13. Operating Characteristics Over Full Ranges of Recommended Operating Conditions(1)(2)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_i	Analog input resistance	See Figure 23.			250	500	Ω
C_i	Analog input capacitance	See Figure 23.	Conversion			10	pF
			Sampling			30	pF
I_{AIL}	Analog input leakage current	See Figure 23.		-1		1	µA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = 3.6 V, $AD_{REFLO} = V_{SSAD}$				5	mA
CR	Conversion range over which specified accuracy is maintained	AD_{REFHI} - AD_{REFLO}		3		3.6	V
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. See Figure 24.				±2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. See Figure 25.				±2	LSB
E_{TOT}	Total error/absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value. See Figure 26.				±2	LSB

(1) $V_{CCAD} = AD_{REFHI}$
(2) 1 LSB = (AD_{REFHI} - AD_{REFLO})/ 2^{10} for the MibADC

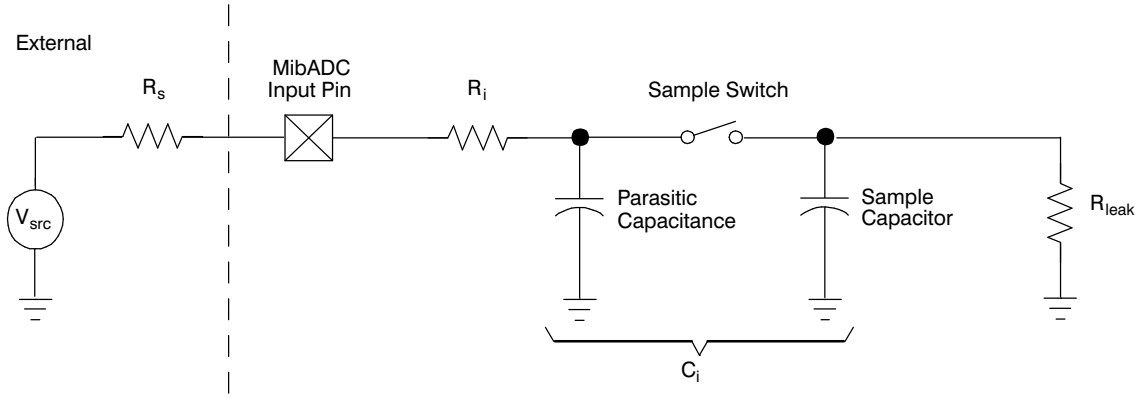


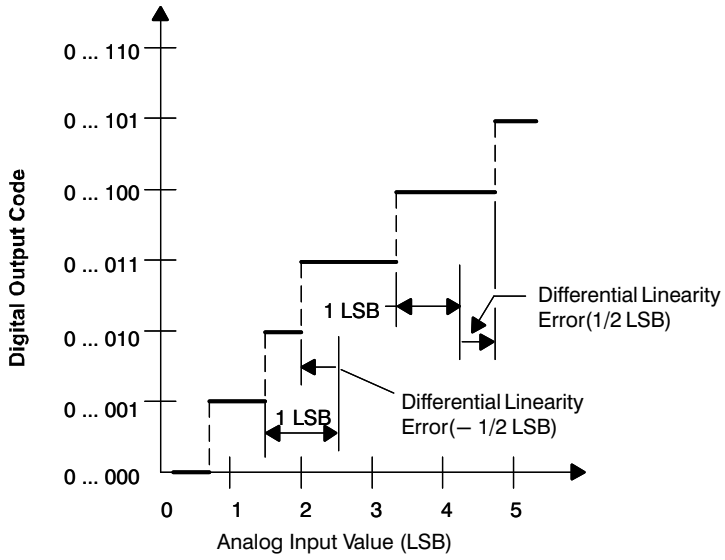
Figure 23. MibADC Input Equivalent Circuit

Multi-Buffer ADC Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05			µs
$t_{d(SH)}$	Delay time, sample and hold time	1			µs
$t_{d(C)}$	Delay time, conversion time	0.55			µs
$t_{d(SHC)}$ (1)	Delay time, total sample/hold and conversion time	1.55			µs

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors; for more details, see the *TMS470R1x Multi-Buffered Analog-to-Digital Converter (MibADC) Reference Guide* (literature number SPNU206).

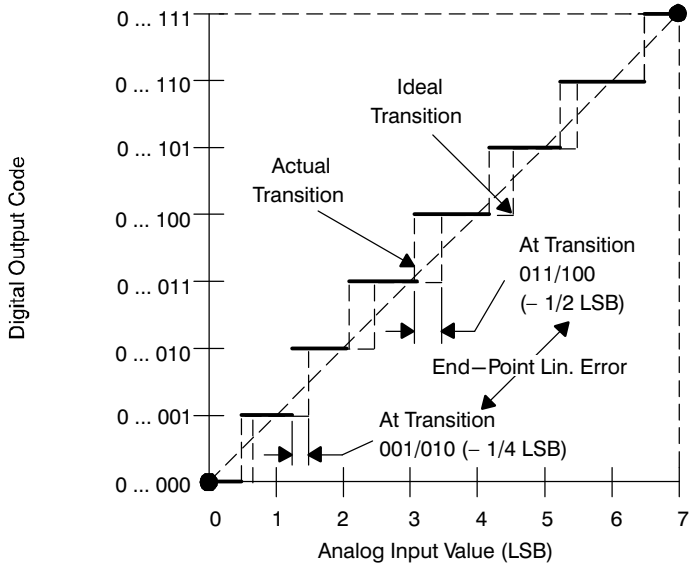
The differential nonlinearity error shown in Figure 24 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 24. Differential Nonlinearity (DNL)

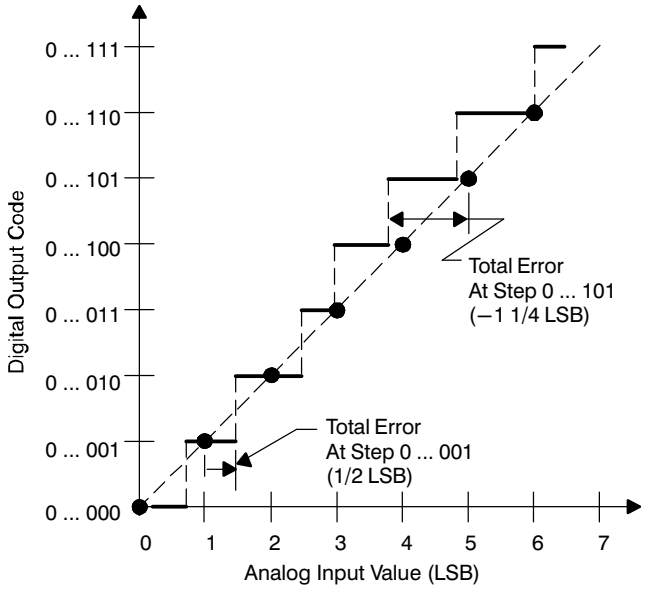
The integral nonlinearity error shown in Figure 25 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 25. Integral Nonlinearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 26 is the maximum value of the difference between an analog value and the ideal midstep value.



A. 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{10}$

Figure 26. Absolute Accuracy (Total) Error

PGE Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	43
$R_{\Theta JC}$	5

PZ Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	48
$R_{\Theta JC}$	5

Revision History

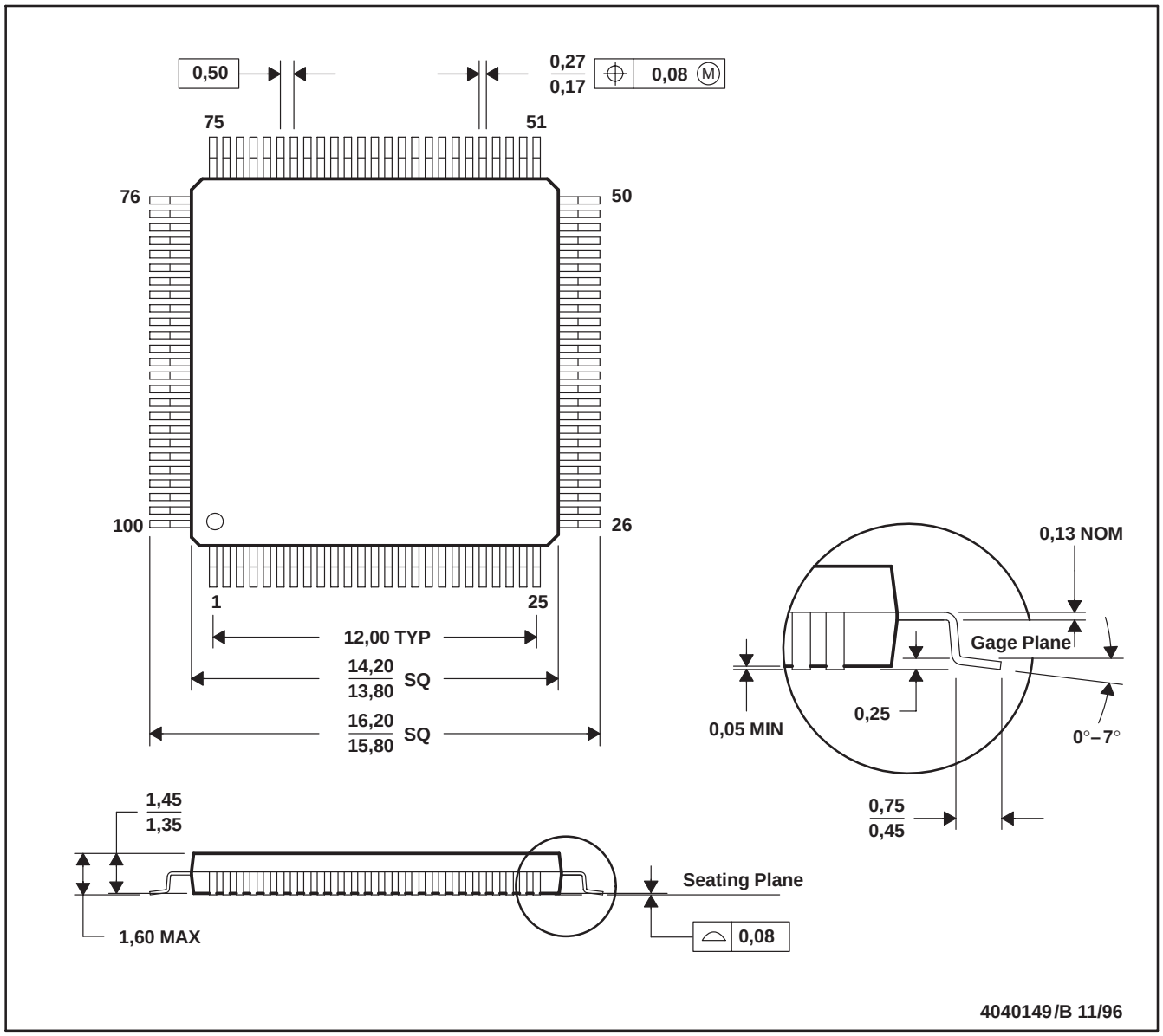
This revision history highlights the changes made to the device-specific datasheet SPNS110 to create the SPNS110A version.

Table 14. Revision History

Page 31	Corrected max value for ICC standby and halt modes in Electrical Characteristics table.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

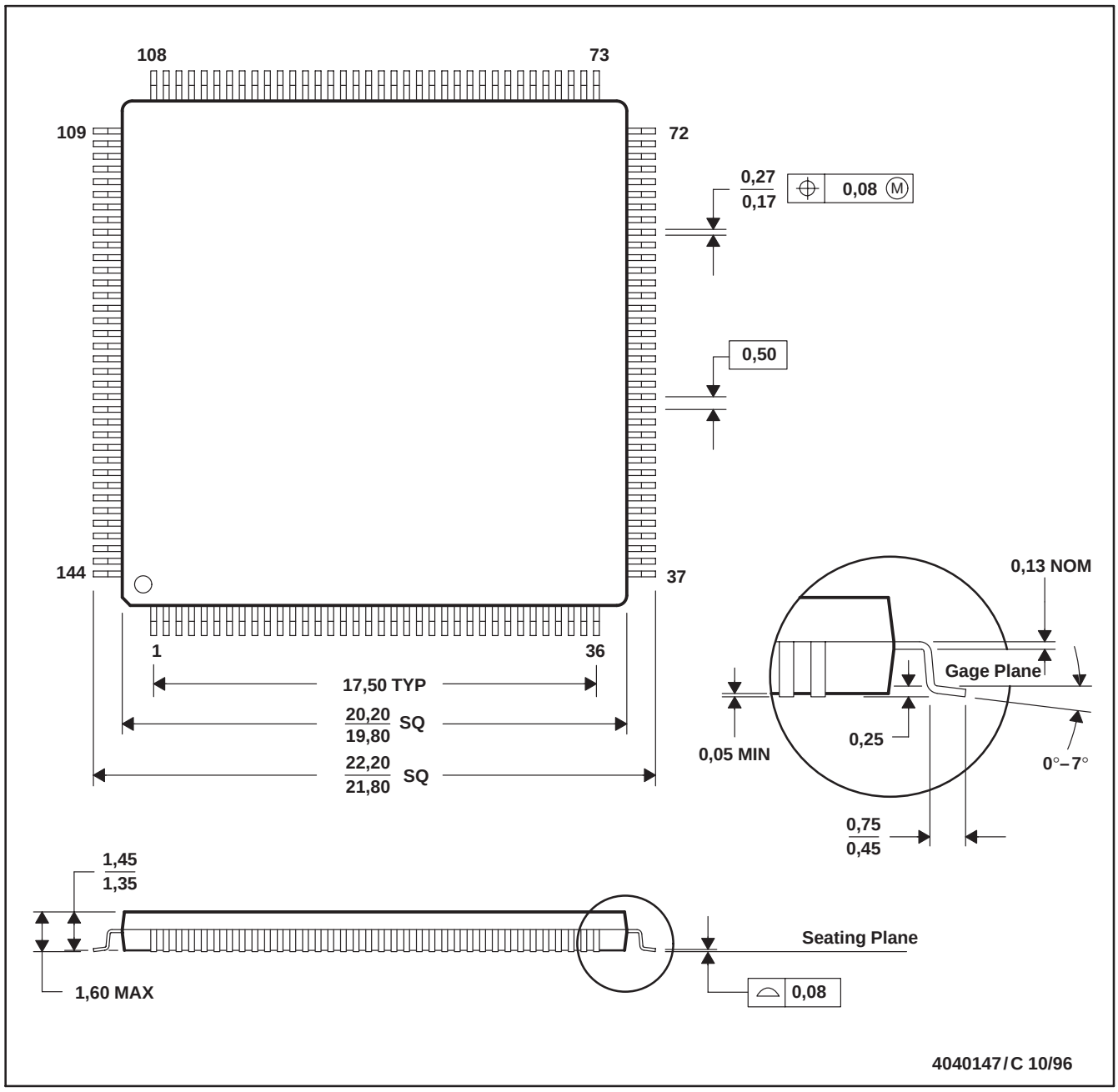
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



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