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MOPS/520

Product Manual

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CONTENTS

1. USER INFORMATION

1.1 About This Manual

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Before contacting JUMP*tec*® technical support, please consult our web site for the latest available product documentation, utilities, and drivers. If the information provided there does not help to solve the problem, contact us by email or telephone. The contact information for technical support in your area is located in Appendix G: Contact Information.

2. INTRODUCTION

2.1 MOPS/520

The ***MOPS/520*** is based on the ÉlanSC520 microcontroller (32-bit Am5x86® CPU). It integrates the complete functionality of motherboard with CPU, System-BIOS, up to 64 MByte SDRAM, keyboard-controller, real time clock and additional peripheral functions like COM1..COM4, LPT1, Floppy-interface, IDE-harddisk-interface, Watchdog, Ethernet access and optional CAN-Bus interface. The system runs with CPU clock speed 100 MHz or 133MHz.

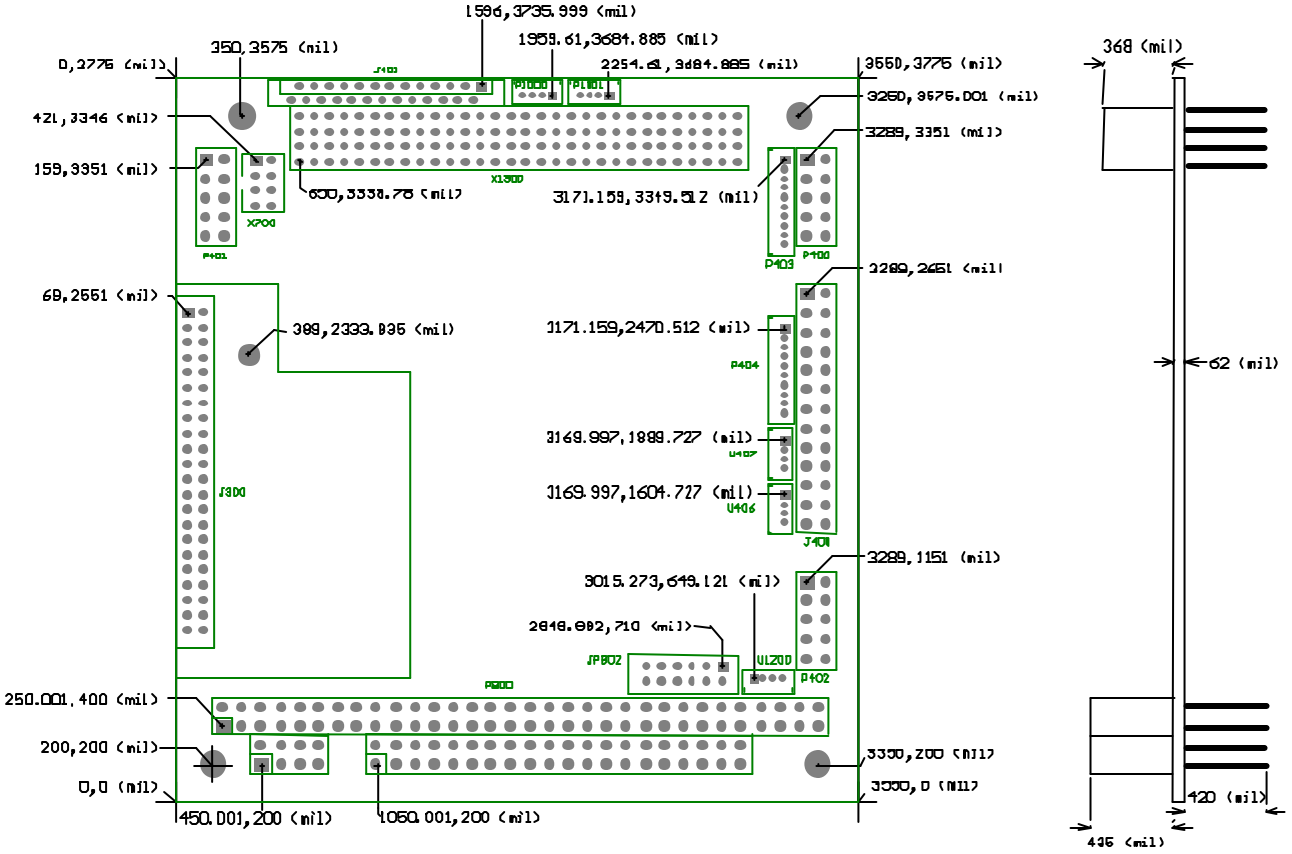
3. SPECIFICATIONS

3.1 Functional Specifications

- Processor Support: 32-bit Am5x86® CPU with 16 KByte write-back-Cache
- Memory: 16/32/64MB SDRAM (onboard)
- BIOS: Phoenix, 256 KByte Flash
- Serial: Three 16550 RS232C, plus one TTL
- Parallel: One port, with ECP/EPP support
- USB: Two ports
- Network: Davicom DM9102A network controller 32-bit Fast Ethernet, 100/10BASET, auto-negotiated
- Bus Expansion: PC/104-Plus ISA/PCI bus connection, 4 ISA PC/104 card drive capability, 4 PC/104*Plus* card drive capability
- IDE: One IDE interface, supporting two drives and JUMPtec® CHIPdisk
- Floppy: Dual floppy support
- Keyboard and PS/2 Mouse
- Real-time Clock: With external Battery-support
- Watchdog Timer
- CAN Bus Interface (optional): Intel® 82527 Controller
- 5V only operation

3.2 Mechanical Specifications

- Mechanical: 3.7" x 3.5 "
- Mounting: 2 pieces of 2x32 pin male and 2x20 pin male connector
- PC/104plus: 4 x 30 pin 2mm connector



The PC/104plus connector is without connector shroud. It's not possible to use a PC/104plus board with connector shroud at top at MOPS/520. This is only a mechanical limitation and does not reduce the functionality of MOPS/520. Please order a module without connector shroud or place MOPS/520 at top at the stack.

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

3.3.3 Supply Current

- Typical: 1.7A
- Maximum: 1.7A

3.3.4 External RTC Battery

- External RTC battery voltage 2.0 - 3.3V (typ. 2.5V)
- External RTC battery quiescent current typ. 5uA

3.4 Environmental Specifications

Temperature:

- Operating: 0 to + 60°C

  The max. case temperature of diode D601 is specified with 70°C. For the detailed location of D601 see Appendix C (section 20.)

- Non-operating: -10 to + 85 ° C
- Humidity: Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

4. CPU, CHIPSET, AND SUPER I/O

4.1 CPU

The ***MOPS/520*** supports the AMD ÉlanSC520 processor with clock speeds up to 133MHz. This is integrated 32-Bit Microcontroller provides following features:

- Synchronous DRAM (SDRAM) controller
- 33 MHz, 32-bit PCI bus Revision 2.2-compliant
- 100-MHz and 133-MHz operating frequencies
- PCI 3.3V/5V tolerance interface
- Low-voltage operation (core V CC = 2.5 V)
- 5-V tolerant I/O (3.3-V output levels)
- 16-Kbyte write-back cache
- Enhanced DMA controller includes double buffer chaining, extended address and transfer counts, and flexible channel routing
- Two 16550-compatible UARTs operate at baud rates up to 1.15 Mbit/s with optional DMA interface
- Programmable interval timer (PIT)
- Real-time clock (RTC) with battery backup capability and 114 bytes of RAM
- Watchdog timer guards against runaway software
- Native support for pSOS, QNX, RTXC, VxWorks, and Windows® CE operating systems
- Enhanced programmable interrupt controller (PIC) prioritizes 22 interrupt levels (up to 15 external sources) with flexible routing

4.2 Chipset

The ***MOPS/520*** contains the ÉlanSC520 micro controller chipset.

4.3 Super I/O

The ***MOPS/520*** contains one Winbond W83977F Super I/O chip.

5. SYSTEM MEMORY

The system memory of the ***MOPS/520*** consists of an onboard SDRAM. It is available in 16, 32, or 64 Megabyte configurations. The memory configuration is set by the factory and cannot be altered.

6. ISA AND PCI BUS EXPANSION

For expansion, the ***MOPS/520*** provides a PC/104-*Plus* socket. This industry standard bus provides both ISA and PCI bus signals. The PC/104-*Plus* standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-*Plus* adapter cards.

6.1 Connectors

J10 is a 64-pin, dual row socket connector, with 0.1" x 0.1" pitch, which implements the standard 8-bit ISA bus signals. J11 is a 40-pin connector of the same style and implements the ISA bus 16-bit expansion signals. All ISA bus signals are supported.

ISA-LOWER/J10					ISA-UPPER/J11			
PIN #	SIGNAL	PIN #	SIGNAL		PIN #	SIGNAL	PIN #	SIGNAL
A1	\IOCHK	B1	GND		C0	GND	D0	GND
A2	SD7	B2	RESDRV		C1	\BHE	D1	\MEMCS16
A3	SD6	B3	VCC (***)		C2	LA23	D2	\IOCS16
A4	SD5	B4	IRQ9		C3	LA22	D3	IRQ10
A5	SD4	B5	-5V		C4	LA21	D4	IRQ11
A6	SD3	B6	DREQ2		C5	LA20	D5	IRQ12
A7	SD2	B7	-12V		C6	LA19	D6	IRQ15(**)
A8	SD1	B8	\WS0		C7	LA18	D7	IRQ14
A9	SD0	B9	+12V		C8	LA17	D8	\DACK0(**)
A10	IOCHRDY	B10	GND (*)		C9	\MEMR	D9	DREQ0 (**)
A11	AEN	B11	\SMEMW		C10	\MEMW	D10	\DACK5
A12	SA19	B12	\SMEMR		C11	SD8	D11	DREQ5
A13	SA18	B13	\IOW		C12	SD9	D12	\DACK6 (**)
A14	SA17	B14	\IOR		C13	SD10	D13	DREQ6 (**)
A15	SA16	B15	\DACK3		C14	SD11	D14	\DACK7 (**)
A16	SA15	B16	DREQ3		C15	SD12	D15	DREQ7 (**)
A17	SA14	B17	\DACK1		C16	SD13	D16	VCC (***)
A18	SA13	B18	DREQ1		C17	SD14	D17	\MASTER (**)
A19	SA12	B19	\REFSH		C18	SD15	D18	GND
A20	SA11	B20	SYSCLK		C19	KEY(*)	D19	GND
A21	SA10	B21	IRQ7					
A22	SA9	B22	IRQ6					
A23	SA8	B23	IRQ5					
A24	SA7	B24	IRQ4					
A25	SA6	B25	IRQ3					
A26	SA5	B26	\DACK2					
A27	SA4	B27	TC					
A28	SA3	B28	ALE					
A29	SA2	B29	VCC (***)					
A30	SA1	B30	OSC					
A31	SA0	B31	GND					
A32	GND	B32	GND					

(*) - Key pin for PC/104; GND for PC/104+ specification

(**) - Not supported on MOPS/520 boards

(***) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

J12 is a quad row socket connector, with 2mm x 2mm pitch, which implements the standard 32-bit PCI bus signals.

6.2 PCI Connector (PC/104+)

Pin	Signal name	Signal Name	Signal Name	Signal Name
	A	B	C	D
1	GND	Reserved	VCC (**)	AD00
2	VCC (**)	AD02	AD01	AD03
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VCC (**)	AD10	GND
7	AD14	AD13	GND	AD12
8	VCC3 (*)	C/BE1	AD15	VCC3 (*)
9	SERR	GND	SB0	PAR
10	GND	PERR	VCC3 (*)	SDONE
11	STOP	VCC3 (*)	LOCK	GND
12	VCC3 (*)	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	VCC3 (*)
14	GND	AD16	VCC3 (*)	C/BE2
15	AD18	VCC3 (*)	AD17	GND
16	AD21	AD20	GND	AD19
17	VCC3 (*)	AD23	AD22	VCC3 (*)
18	IDSEL0 (AD20)	GND	IDSEL1 (AD21)	IDSEL2 (AD22)
19	AD24	C/BE3	VI/O	IDSEL3 (AD23)
20	GND	AD26	AD25	GND
21	AD29	VCC (**)	AD28	AD27
22	VCC (**)	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	VCC (**)	GNT0
25	GNT1	VI/O	GNT2	GND
26	VCC (**)	CLK0	GND	CLK1
27	CLK2	VCC (**)	CLK3	GND
28	GND	INTD	VCC (**)	RST
29	+12V	INTA	INTB	INTC
30	-12V	Reserved	Reserved	Reserved

(*) - NOT SUPPORTED ON MOPS/520

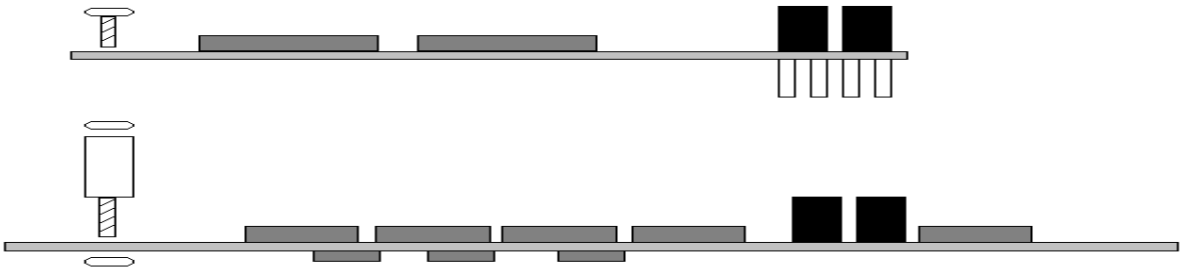
(**) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

FOR SIGNAL DESCRIPTION AND PERIPHERAL DRIVER CURRENT, REFER TO THE PC/104+ SPECIFICATION.

6.3 Adapter Card Mounting

PC/104 and PC/104-*Plus* adapter cards are mounted in a "stack-through" manner. Adapter cards are designed with plugs on their undersides that mate with the PC/104 socket connectors of ***MOPS/520***. PC/104 adapters can support the socket connector version on their topside and allow further "stacking" of adapters.



6.4 I/O Address Mapping Limitation

Only I/O addresses below 400h are mapped to the external ISA respectively PC104 bus. All higher I/O addresses are directed to PCI.

7. UNIVERSAL SERIAL BUS (USB) INTERFACE

The ***MOPS/520*** comes with two USB ports and further expansion may be achieved by adding external hubs. Technically, up to 127 individual USB peripherals can be connected at one time.

7.1 USB1 and USB2 Connector

PIN	PIN FUNCTION
1	+5V
2	USB-
3	USB+
4	GND

The power contacts on PIN 1 and 4 are only usable for internal USB devices.
It is strictly recommended to use a fuse for power on external USB connectors.

8. SERIAL COMMUNICATION INTERFACE

The ***MOPS/520*** has four 16550-compatible serial ports, COMA, COMB, COMC and COMD. The line drivers used for COMA through COMC conform to the IEEE RS-232C standard. COMD is a TTL-level interface.

8.1 Connectors

COMA, COMB, COMC (RS232C) AND COMD (TTL)				
PIN	**SIGNALNAME**	**IN / OUT**	**DSUB-25 (NEED ADAPTER)**	**DSUB-9 (NEED ADAPTER)**
1	DCD	In	8	1
2	DSR	In	6	6
3	RxD	In	3	2
4	RTS	Out	4	7
5	TxD	Out	2	3
6	CTS	In	5	8
7	DTR	Out	20	4
8	RI	In	22	9
9	GND	--	7	5
10	VCC (*)	--	--	--

For signal descriptions, please refer to additional literature.

(*) - To protect the external powerlines of peripheral devices the customer has to take care about:

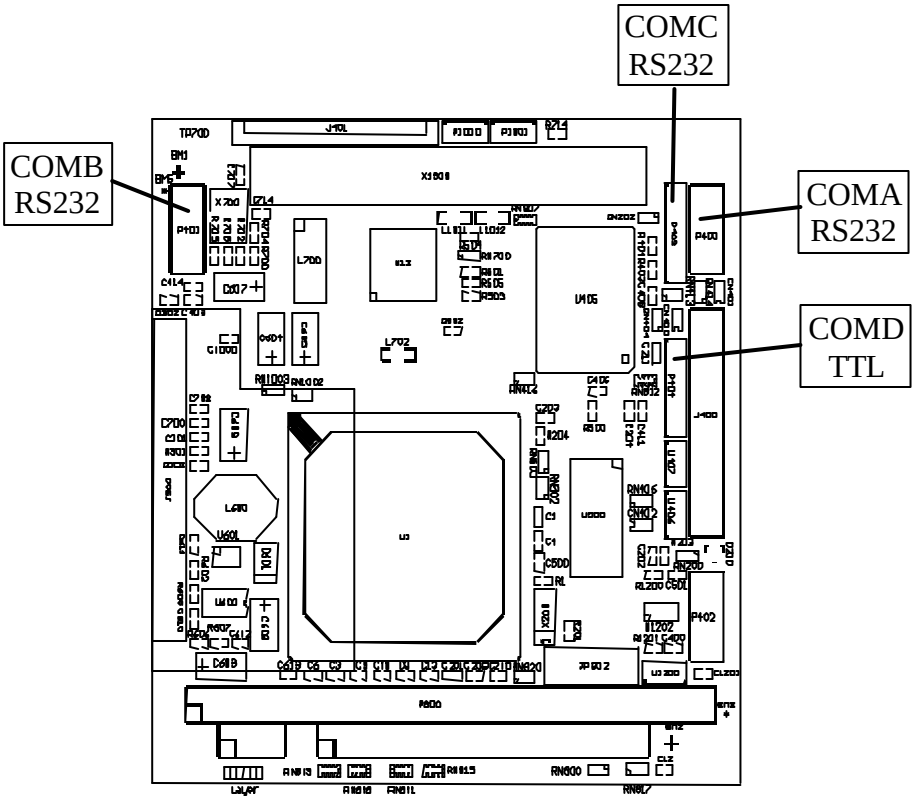
- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

The serial ports are completely compatible with the serial port implementation used on the IBM Serial Adapter.

8.2 Configuration

COMA and COMB can be set to several I/O-addresses and IRQs in the setup. COMC and COMD are fix-mapped to the addresses and IRQs. See the table below for more information.

SERIAL PORT	POSSIBLE I/O-ADDRESSES	POSSIBLE IRQS
COMA	3F8h, 2F8h, 3E8h, 2E8h	3, 4, 10
COMB	3F8h, 2F8h, 3E8h, 2E8h	3, 4, 11
COMC	3F8h	4
COMD	2F8	3



Please Note: Most OS detect the serial port with the I/O-address 3F8h as COM1 and 2F8h as COM2. Therefore, if COMC and COMD are enabled they will be detected as COM1 and COM2.

8.3 Limitations

The SC520 integrated serial ports (serial port C and D on the MOPS/520) show two deviations from the standard UART behaviour:

The delta ring indicator bit in the modem status register (bit 2) is only set when the ring indicator signal has changed from an active to an inactive state since the last time the modem status register was read.

Usually this bit is set for RI changes from inactive to active as well.

In 16550 compatible mode a received data interrupt is generated when the very first data byte of a continuous data stream is placed in FIFO. This error only occurs for the first character of a continuous data stream received by the UART. Following the FIFO time-out interrupt for the first character received, the remainder of the data stream will be indicated according to the trigger value set in the RFRT bits of the UART FIFO control registers.

9. PARALLEL COMMUNICATION INTERFACE

The ***MOPS/520*** supports one enhanced parallel port. ECP and EPP modes are supported.

9.1 Connectors

PARALLEL PORT LPT 1				
PIN	**SIGNALNAME**	**FUNCTION**	**IN / OUT**	**DSUB-25 (NEED ADAPTER)**
1	/Strobe		Out	1
3	Data 0		I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7		I/O	9
19	/ACK		in	10
21	BUSY		in	11
23	PAPER out		in	12
25	SEL out		in	13
2	/AUTOFD		out	14
4	/ERROR		in	15
6	/INIT		out	16
8	SEL in		out	17
26	VCC (*)	+ 5 V	--	NC
10,12	GND	Signal Ground	--	18 - 25
14,16	GND	Signal Ground	--	18 - 25
18,20	GND	Signal Ground	--	18 - 25
22,24	GND	Signal Ground	--	18 - 25

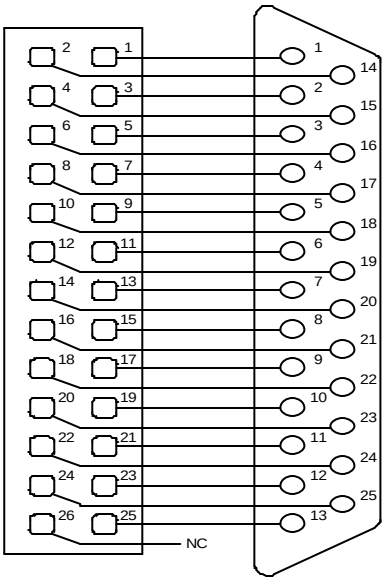
For signal description please refer to additional literature.

(*) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

The Centronics printer interface can be programmed via the system setup menu. Refer to the peripheral setup for more information. The parallel port is completely compatible with the parallel port implementation used in the IBM PS-II-Parallel Adapter.

An adapter cable may be used to change from the 26-pin header style of the ***MOPS/520*** to the more common 25-pin female D-sub.



26-pin Header to 25-pin D-Sub conversion

9.2 Configuration

The ***MOPS/520*** parallel ports are fully bi-directional. The bi-directional functions are compatible with those of a PS/2 style parallel port. This functionality is always available and does not conflict with normal printer use. The parallel port mode, I/O addresses, and IRQs are defined in the BIOS Setup utility.

9.3 Limitations

Due to chipset limitations, parallel port mode ECP as well as parallel port base address 3BCh (in any mode) cannot be used when a PCI video adapter is installed on the system. With ISA video adapters these restrictions do not apply

10. FRONT PANEL INTERFACE

The Front Panel Interface consists of the following: Keyboard, Reset, Battery, Speaker.

10.1 Connector

PIN	SIGNAL NAME	FUNCTION	5-PIN DIODE KEYBOARD ADAPTER	6-PIN MINIDIN KEYBOARD ADAPTER (PS2)
1	SPKR	Speaker output		
2	GND	Ground		
3	RESIN	Reset input 1		
4	/KLOCK	Keyboard lock		
5	KDATA	Keyboard data	2	1
6	KCLK	Keyboard clock	1	5
7	GND	Ground	4	3
8	VCC (*)	+5V	5	4
9	VBAT	VBAT input (max. 3,3V)		
10	POWERGOOD	Reset input 2		

(*) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

/KLOCK (keyboard lock)

- Input on CPU modules
- Output on any other module
- Input to the keyboard controller: input port 1 bit 7

RESIN (reset input 1)

- Input on CPU modules
- Open collector output on all other modules
- When the power good goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. This pin can also be used as a low active hardware reset for modules.

SPKR (speaker output)

- Open collector output on modules that can drive a loudspeaker
- Input on modules which connects an 8-Ohm loudspeaker to this pin.
- An 8-Ohm loudspeaker is connected between SPEAKER and GND. Only one loudspeaker should be connected to this pin. Usually only the CPU drives this pin, however other modules can also use this signal to drive the system loudspeaker.

KDATA (keyboard data)

- Bi-directional I/O pin on CPU modules
- Keyboard data signal

KCLK (keyboard clock)

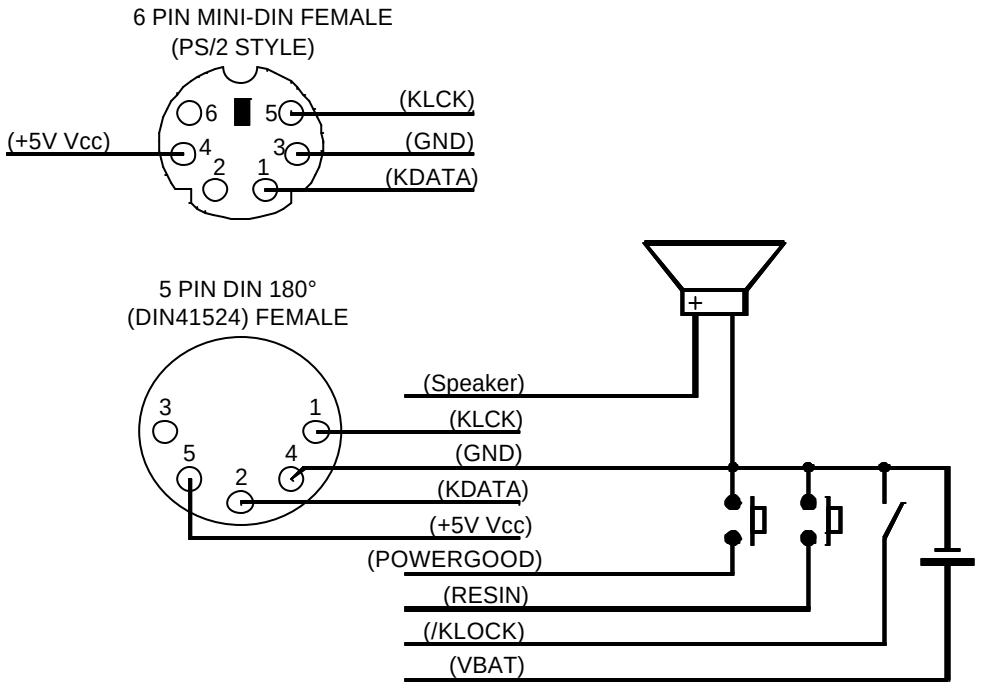
- Bi-directional I/O pin on CPU modules
- Keyboard clock signal

VBAT (system battery connection)

- This pin connects a system battery to all modules.
- The battery voltage has to be higher than 2.0V and lower than 3.3V. A 3V battery is recommended.
- Note that there is no battery needed to hold the CMOS-setup data. Your configuration concerning hard disks, floppy drives etc. is automatically saved in an onboard FRAM. However, the battery is necessary to serve the CMOS date and time while power consumption is turned off.

POWERGOOD (reset input 2)

- Input on CPU modules
- Open collector output on all other modules
- When power good goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. This pin can also be used as a low active hardware reset for modules.



11. FLOPPY DISK INTERFACE

The floppy disk interface can support one 3.5” drive, using the adapter cable ADA-Floppy 2, (part number 96001-0000-00-0). Supported drive capacities are 720K, 1.44M, or 2.88M.

11.1 Connector

PIN	Signal	Function	Pin	Signal	Function
1	VCC (*)	+ 5V	2	IDX	Index
3	VCC (*)	+ 5V	4	DS0	Drive select 0
5	VCC (*)	+ 5V	6	/DCHNG	Disk change
7	NC	-	8	NC	-
9	NC	-	10	Mo0	Motor on
11	NC	-	12	DIR	Direction select
13	NC	-	14	STEP	Step
15	GND	Ground	16	WD	Write data
17	GND	Ground	18	WG	Write gate
19	GND	Ground	20	TR00	Track 00
21	GND	Ground	22	WP	Write protect
23	GND	Ground	24	RD	Read data
25	GND	Ground	26	SIDE	Side one select

(*) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

For signal descriptions, please refer to additional literature.

11.2 Configuration

The drive type must be specified using the BIOS Setup utility. The 3.5" drive type can be 720KB, 1.44MB, 2.44MB, or NONE. The floppy disk interface can be disabled in BIOS Setup.

12. IDE INTERFACE

The ***MOPS/520*** contains one IDE interface capable of driving two hard disks. When two devices are connected to a single adapter, they are connected in a typical Master/Slave, daisy chain fashion.

12.1 Connector

IDE connector is a 44-pin, dual in-line, 2mm pitch, and male header.

One or two IDE drives may be connected to the header by using the appropriate flat ribbon cable. The first drive must be configured as the master; the second drive (at the end of the cable) must be configured as the slave. Consult the disk drive manual for instructions on this task.

IDE CONNECTOR FOR 2.5 " HARD DISK			
PIN	**SIGNAL**	**PIN**	**SIGNAL**
1	/RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	NC
21	NC	22	GND
23	/IOW	24	GND
25	/IOR	26	GND
27	NC	28	BALE
29	NC	30	GND
31	IRQ14	32	/IOCS16
33	SA1	34	NC
35	SA 0	36	SA2
37	/CS0	38	/CS1
39	/HDLED	40	GND
41	VCC	42	VCC
43	GND	44	NC

13. ETHERNET INTERFACE

The ***MOPS/520*** on-board Ethernet interface is based on the Davicom DM9102A PCI Fast Ethernet Controller. This network controller supports a 10/100Base-T interface. The device auto-negotiates whether a 10Mbit/sec or 100Mbit/sec connection is to be used.

All major network operating systems, and several real-time and embedded operating systems support the interface.

The DM9102A provides the following features:

- Integrated Fast Ethernet MAC, Physical Layer and transceiver in one chip
- Compliance with PCI specification 2.2
- PCI bus master architecture
- EEPROM 93C46 interface supports node ID access configuration information
- Compliance with IEEE 802.3u 100Base-TX and 802.3 10Base-T
- Compliance with IEEE 802.3u auto-negotiation protocol for automatic link type selection
- Full Duplex/Half Duplex capability
- Support IEEE 802.3x Full Duplex Flow Control
- Digital clock recovery circuit using advanced digital algorithm to reduce jitter
- High performance 100Mbps clock generator and data recovery circuit
- Provides Loopback mode for easy system diagnostics

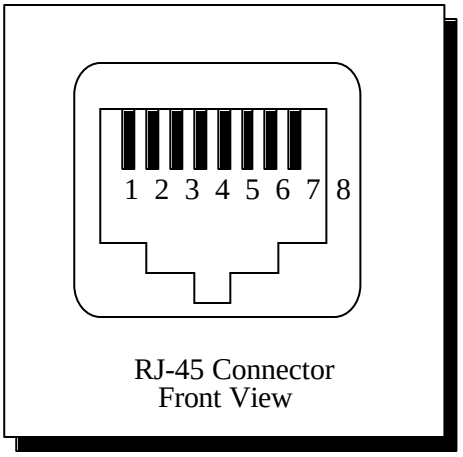
13.1 Configuration

The on-board PCI Ethernet interface is configured by the BIOS configuration manager. It will be assigned to an available I/O and IRQ location.

13.2 Connectors

The 10/100Base-T connector is a standard 8-pin RJ45 jack

13.2.1 RJ45 Pinout



RJ-45 Connector
Front View

PIN#	SIGNALNAME	FUNCTION	IN/OUT
1	TXD+	100/10BASE-T Transmit	Differential Output
2	TXD-	100/10BASE-T Transmit	Differential Output
3	RXD+	100/10BASE-T Receive	Differential Input
4	NC	Unused Pin	
5	NC	Unused Pin	
6	RXD-	100/10BASE-T Receive	Differential Input
7	NC	Unused Pin	Output
8	NC	Unused Pin	Output

TXD+, TXD- Differential output pair drives 10 and 100Mb/s Manchester encoded data to the 100/10BASE-T transmit lines.

RXD+, RXD- Differential input pair receives 10 and 100Mb/s Manchester encoded data from the 100/10BASE-T receive lines.

13.3 Ethernet Technical Support

Many problems can be solved with the latest drivers for the DAVICOM DM9102A controller. **JUMP*tec*®** provides you with the latest *tested* drivers, which might be quite different from the newest ones. Therefore, please visit the DAVICOM web page for driver updates.
For further technical support, contact either **JUMP*tec*®** or get support information and download software updates from DAVICOM World Wide Web server.

DAVICOM World Wide Web server

Home: http://www.davicom.com.tw/
Drivers: http://www.davicom.com.tw/download/download_driver.asp

Before contacting **JUMP*tec***® for technical support, please be prepared to provide as much of the following information as possible.

1) Adapter type
2) Adapter configuration
3) - I/O Base, Memory Base, I/O or memory mode enabled, IRQ, and DMA channel
   - Configured for media auto-detect or specific media type (which type).
   (Record this information from the driver's sign-on message if possible.)
4) Computer System's Configuration
   - BIOS (make and version)
   - System make and model
   - CPU (type and speed)
   - System RAM
5) Software
   – DM9102A driver and version
   - Your network operating system and version
   - Your system's OS make/version (MS-DOS, Novell's DOS, Win95, WFWG, etc.)
   - Version of all protocol support files
   - Frame types supported by you server
6) Contents of your configuration files
   - CONFIG.SYS
   - AUTOEXEC.BAT
   - PROTOCOL.INI
   - NET.CFG FILE
   - WINDOW'S SYSTEM.INI (if using Windows client)
   - AUTOEXEC.NCF file
   - or similar
7) Any Error Message displayed

14. POWER

14.1 Power Connector

POWER CONNECTOR	
PIN	**SIGNAL**
1	GND
2	+5V
3	VBAT
4	+12V
5	-5V
6	-12V
7	GND
8	+5V

14.2 Power Pins

The ***MOPS/520*** is a +5 V only module. Nevertheless the power connector offers the possibility to supply with the additional voltages +12V, -12V and -5V, which may be necessary for other boards in the PC/104 system. The power consumption of all available power pins on the ***MOPS/520*** is limited to 5A in total (1A per pin, with 2 pins on the power connector, 2 pins on the XT-bus and 1 pin on the AT-bus) and at GND up to 8A. Systems consuming more then 2A shouldn't be served over the power connector only. Systems consuming more then 5A must provide power supply through an additional connector on another board.

The MOPS/520 is not a replacement for a backplane. It is strictly recommended to use all Power Pins on the PC/104 connector for power supply of the MOPS/520 and additional I/O cards. It is not acceptable to use only the power pins of the PC/104plus PCI connector for power supply of the full PC/104 stack.

14.3 VBAT (system battery connection)

This pin connects a system battery to all modules.

The battery voltage has to be higher than 2.0V and lower than 3.3V. A 3V battery is recommended.

Please note that there is no battery needed to hold the CMOS-setup data. Your configuration concerning hard disks, floppy drives etc. is automatically saved in an onboard FRAM. Nevertheless the battery is necessary to serve the CMOS date and time while power consumption is turned off.

15. WATCHDOG TIMER

The watchdog timer feature of the ***MOPS/520*** provides a means to insure the integrity of system operation. The timer is integrated into the Élan™SC520 Microcontroller. When enabled, system software must refresh the timer within the specified timeout period or the timer will be triggered. The timer can be programmed to either reset the system or initiate a Non-Maskable Interrupt (NMI) when triggered.

15.1 Watchdog BIOS Interface

The watchdog timer may be enabled or disabled in BIOS Setup or through an Interrupt 15h BIOS function call. The Interrupt 15h Watchdog functions have the following calling conventions:

Watchdog init	Int 15h	00h
Input:	AH = E0h AL = 00h BX = timeout in 0.2 sec increments CX = delay in 0.2sec increments DX = watchdog action (0 = reset, 1 = NMI)	
Output:	None	
Description:	This function is a public JUMP*tec*® INT15h extension used to init the watchdog on JUMP*tec*® boards.	

Watchdog trigger	Int 15h	01h
Input:	AH = E0h AL = 01h	
Output:	None	
Description:	This function is a public JUMP*tec*® INT15h extension used to trigger the watchdog on JUMP*tec*® boards.	

The function *Init watchdog* must be called only once. The two parameters *timeout time* and *trigger event* must be set. The watchdog must be reset during the *timeout time* with the *trigger watchdog function*. Otherwise a RESET or NMI will occur depending on *trigger event*

The trigger and the delay time can be set in steps of 0.2 sec.

The theoretical maximum values are:

- Timeout time 65535*0.2sec. = 13107s ≅ 3h 38min
- Delay time 32767*0.2sec. = 6553s ≅ 1h 49min

NOTE:

The limits above apply to the Int 15h interface. Due to internal limitations of the MOPS/520 Watchdog, only the following delay/timeout values can actually be set:

0.5s, 1s, 2s, 4s, 8s, 16s, 32s

The interface will internally round other settings to the actually possible time values.

INIT WATCHDOG (INT 15H, AH=E0H)		
Called with	AX	E000h
	BX	**timeout time** BX = 0 ⇨ watchdog off. BX_{max} = 0FFFFh
	CX	**delay time** CX = 0 ⇨ no delay. CX_{max} = 07FFFh
	DX	**trigger event** DX = 0 ⇨ RESET, DX = 1 ⇨ NMI
Returns	no	

EXAMPLE

```
mov   ax,0E000h    ; Watchdog set
mov   bx,5         ; 5*0,2s = 1s Timeout
mov   cx,5         ; 5*0,2s = 1s Delay
mov   dx,0         ; after Timeout and Delay generate RESET
int   15h
```

16. CAN-BUS

The CAN-Bus on the ***MOPS/520*** Boards is based on INTEL® 82527 controller.

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backward compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

A PC82C251 from PHILIPS acts as an interface to the physical bus. This is a CAN transceiver for 24 V systems.

16.1 Connector

Pin	Pin function
1	CAN_L
2	CAN_H
3	VCC (*)
4	GND

(*) - To protect the external powerlines of peripheral devices the customer has to take care about:

- that the wires have the right diameter to withstand the maximum available current
- that the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

17. THE JIDA STANDARD

JIDA is the abbreviation for **JUMP*tec*®** Intelligent Device Architecture.
Every board with onboard BIOS extension shall support the following function calls, which supply information about the board. JIDA functions are called via Interrupt 15h with AH=EAh, AL=function number, DX=4648h (security word), CL=board number (starting with 1).

The interrupt will return with CL#0 if a board with the number specified in CL does not exist.

CL will be equal to 0 if the board number exists. In this case, the content of DX is used to determine if the operation was successful. DX=6B6Fh indicates successful operation; any other value indicates an error.

To get information about the installed boards following the JIDA standard, the following procedure is recommended:

Call "Get Device ID" with CL=1. The name of the first device installed will be returned.
If result was "Board exists" (CL=0), increment CL and call "Get Device ID" again.
Repeat until result is "Board not present" (CL#0).

You now know the names of all boards within your system that follow the JIDA standard. More information about a specific board may then be obtained by calling the appropriate inquiry function with the board's number in CL.

NOTE: Association between board and board number may change due to configuration changes. Do **not rely on any association between board and board number**. Always use the procedure described in the preceding paragraph first, to determine the association between board and board number.

The manual and sample code for the JIDA is available from our web page at www.jumptec.de.

18. APPENDIX A: SYSTEM RESOURCE ALLOCATIONS

18.1 I/O Port Assignments

Devices on the MOPS/520 use I/O addresses common to the PC/AT. Note: Only I/O addresses below 400h are mapped to the external ISA respectively PC104 bus. All higher I/O addresses are directed to PCI.

18.2 Interrupt Request Lines

The following table describes the allocation of the 16 hardware interrupt lines for the ***MOPS/520***. The allocations shown are typical. Many subsystems that use the hardware interrupt lines can use alternate lines if desired. These alternate choices are selectable via the BIOS Configuration Register.

IRQ #	PRIMARY USE	AVAILABLE
0	Timer0	---
1	Keyboard	---
2	Cascade	---
3	COM2	Note (1)
4	COM1	Note (1)
5	CAN-Bus	Note (1)
6	Floppy	---
7	LPT1	---
8	Clock/Calendar	---
9	Available	Yes
10	COM 3	Note (1)
11	COM 4	Note (1)
12	PS/2 Mouse	Note (1)
13	Numeric-processor	---
14	IDE Channel 1	---
15	Not available	Not available

Note (1) If serial ports, PS/2 mouse or CAN controller are disabled via system bios, these interrupts are available for other devices.

18.3 Direct Memory Access Channels

DMA #	USED FOR	AVAILABLE
1		**Yes**
2	**Floppy**	**No**
3		**Yes**
5		**Yes**

18.4 Upper Memory Area Map

UPPER MEMORY	USED FOR	AVAILABLE
A0000h – BFFFFh	VGA Memory	No
C0000h – CFFFFh	VGA BIOS	No
D0000h – DFFFFh		Yes
E0000h – F0000h	System BIOS	No

19. APPENDIX B: BIOS OPERATION

The ***MOPS/520*** is equipped with a Phoenix BIOS, which is located in a Flash EPROM onboard. This device has 8bit wide access. Faster access (16bit) is provided by the shadow RAM feature (default).

19.1 The Setup Guide

With the Phoenix BIOS Setup program, you are able to modify BIOS settings and control the special features of the computer. The setup program uses a number of menus for turning the special features on or off, as well as making changes.

General Information

To start the Phoenix BIOS setup utility press <F2> during the string Press <F2> to enter, setup is displayed during bootup. The Main Menu will be displayed.

The Menu Bar

The Menu Bar at the top of the window lists all the different menus. Use the left/right arrows to make a selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selection or exit the current menu. The table below describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General help window
<Esc>	Exit this menu
← or → Arrow key	Select a different menu
↑ or ↓ Arrow key	Move cursor up and down
<Tap> or <Shift-Tap>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of current window
<PgUp> or <PgDn>	Move cursor to next or previous page
<F5> or <->	Select the previous value for the current field
<F6> or <+> or <Space>	Select the next value for the current field
<F9>	Load default configuration values for this menu
<F10>	Save and Exit
<Enter>	Execute command or select submenu
<Alt-R>	Refresh screen

To select an item, simply use the arrow key to move the cursor to the field you want. Then use the plus and minus keys to select a value for that field. The Save Value commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub menu, use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A pointer (▸) marks all sub menus.

The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It is updated as the cursor is moved to each field.

The General Help Window

Pressing <F1> or <Alt-F1> on any menu brings up the General Help Window that describes the legend keys and their alternates. Press <Esc> to exit the General Help Window.

19.1.1 The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Option	Description
System Time	HH:MM:SS	Set the system time. Use <Enter to move to MM or SS.
System Date	MM/DD/YYYY	Set the system date. . Use <Enter to move to DD or YYYY.
Legacy Diskette A	360 kB, 5 ¼ " 1.2 MB, 5 ¼ " 720 kB, 3 ½ " **1.44/1.25 MB, 3 ½ "** 2.88 MB, 3 ½ " Not Installed Disabled	Select the type of floppy disk drive installed in the system.
‣ Primary Master	autodetected drive	Displays result of PM autotyping.
‣ Primary Slave	autodetected drive	Displays result of PS autotyping.
‣ Memory Shadow	Sub menu	Opens Memory Shadow Menu
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory	N/A	Displays amount of extended memory detected during bootup.

Selecting one of the Master or Slave sub menus displays a menu similar to this:

Feature	Option	Description
Type	None User **Auto** CD-ROM	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies the hdd information. Auto = Autotyping, the drive itself supplies the information. CD-ROM = CD-ROM drive.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity (CHS)	N/A	Displays the calculated size of the drive in CHS
Total Sectors*	N/A	Total number of sectors in LBA mode
Maximum Capacity (LBA)*	N/A	Displays the calculated size of the drive in LBA

Multi-Sector Transfer	Disabled Standard 2 sectors 4 sectors 8 sectors **16 sectors**	Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block.
LBA Mode Control	Disabled **Enabled**	Enabling LBA causes Logical Block Addressing to be used in place of CHS.

*Only if LBA Mode Control enabled

Memory Shadow sub menu:

Feature	**Option**	**Description**
Video Shadow	Disabled **Enabled**	Enables/disables shadowing of video ROM
C800 – CFFF	**Disabled** Enabled	Accesses to this upper memory region go to the ISA bus if 'Disabled' or to local memory if 'Enabled'. NOTE: This option is not displayed if VGA BIOS exceeds 32kB! In that case this region is shadowed automatically.
D000 – D7FF	**Disabled** Enabled	See above.
D800 – DFFF	**Disabled** Enabled	See above.

19.1.2 The Advanced Menu

Selecting "Advanced" from the menu bar displays this menu:

Feature	**Option**	**Description**
‣ Advanced Chipset Control	Sub menu	Opens Advanced Chipset Control sub menu.
‣ PCI Configuration	Sub menu	Opens PCI Advanced sub menu.
PNP OS installed	Yes **No**	If your system has a PNP OS (e.g. Win95) select 'Yes' to let the OS configure PNP devices not required for boot. 'No' makes the BIOS configure them.
Reset Configuration Data	**No** Yes	'Yes' erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select 'Yes' when required to restore the manufacturer's defaults.
PS/2 Mouse	Disabled Enabled **Auto**	PS/2 mouse configuration.

‣ Keyboard Features	Sub menu	Opens Keyboard Features sub menu.
‣ I/O Device Configuration	Sub menu	Opens I/O Device Configuration sub menu.
Large Disk Access Mode	**DOS** Other	Select 'DOS' if you have DOS. Select 'Other' if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Halt On Errors	Yes **No**	Determines if post errors cause the system to halt.

Advanced Chipset Control sub menu:

Feature	**Option**	**Description**
CPU Speed	100 MHz **133 MHz**	Select CPU frequency.
Cache Mode	**Write Back** Write Through	Select SC520 L1 cache mode.
CAS latency	**3T** **2T**	Select CAS latency.
RAS to CAS delay	2T **3T** 4T	Select RAS to CAS delay.
RAS Precharge time	2T **3T** 4T 6T	Select RAS precharge time.
Refresh cycle time	7.8 us **15.6 us** 31.2 us 62.5 us	Select SDRAM refresh cycle time.
SDRAM buffer	Disabled **Enabled**	The integrated SDRAM read/write buffer increases overall system performance.
ISA bus cycle duration:	400ns **800ns** 1.2us 2us	Set the duration of a complete ISA bus cycle.

PCI Configuration sub menu:

Feature	**Option**	**Description**
PCI concurrent mode	Disabled **Enabled**	In concurrent mode direct PCI to PCI transfers do not require gaining ownership of the CPU-memory host bus. Thus PCI transfers are accelerated.

Park PCI on CPU*	**Enabled** Disabled	'Enabled': The PCI bus is parked on the CPU after PCI transaction. 'Disabled': The PCI bus is parked on the last PCI master.
CPU PCI master priority*	**1**, 2, 3	The CPU is granted the PCI bus after the selected number of external PCI master cycles.
Delay Transaction*	**Disabled** Enabled	'Enabled' maximizes PCI bus efficiency by freeing up the bus while initial SDRAM read is issued.
Host-Pci Write Buffer*	**Disabled** Enabled	Maximizes host write accesses to PCI.
▸ PCI Device, Slot #1	Sub menu	Opens sub menu to configure slot 1 PCI device
▸ PCI Device, Slot #2	Sub menu	Opens sub menu to configure slot 2 PCI device
▸ PCI Device, Slot #3	Sub menu	Opens sub menu to configure slot 3 PCI device
▸ PCI Device, Slot #4	Sub menu	Opens sub menu to configure slot 4 PCI device
PCI IRQ line 1	Disabled **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	Select IRQ for PIC interrupt INTA. Select 'Auto' to allow BIOS to assign the IRQ.
PCI IRQ line 2	See above	Select IRQ for PIC interrupt INTB. Select Auto to let the BIOS assign the IRQ.
PCI IRQ line 3	See above	Select IRQ for PIC interrupt INTC. Select Auto to let the BIOS assign the IRQ.
PCI IRQ line 4	See above	Select IRQ for PIC interrupt INTD. Select Auto to let the BIOS assign the IRQ.
▸ PCI/PNP ISA UMB Region Exclusion	Sub menu	Opens UMB Region Exclusion sub menu.
▸ PCI/PNP ISA IRQ Resource Exclusion	Sub menu	Opens IRQ Exclusion sub menu.
Assign IRQ to PCI VGA	**Yes** No	Actually, most graphic cards do not need an IRQ assigned, however Win98 2nd Edition doesn't work properly if no IRQ is assigned.

*Only visible if PCI concurrent mode is set to Enabled.

PCI Device, Slot #X sub menu:

Feature	**Option**	**Description**
Option ROM Scan	Disabled **Enabled**	Initialize device expansion ROM
Enable Master	Disabled	Enables device in slot as a PCI bus master.

	Enabled	Not every device can function as a master. Check your device documentation.
Latency Timer	20h, **40h**, 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

PCI/PNP ISA UMB Region Exclusion sub menu:

Feature	**Option**	**Description**
C800 - CBFF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
CC00 - CFFF	See above	See above
D000 – D3FF	See above	See above
D400 – D7FF	See above	See above
D800 - DBFF	See above	See above
DC00 - DFFF	See above	See above

PCI/PNP ISA IRQ Exclusion sub menu:

Feature	**Option**	**Description**
IRQ3	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	See above	See above
IRQ5	See above	See above
IRQ7	See above	See above
IRQ9	See above	See above
IRQ10	See above	See above
IRQ11	See above	See above
IRQ14 (only visible if IDE disabled)	See above	See above
IRQ15	See above	See above

Keyboard Features sub menu:

Feature	**Option**	**Description**
NumLock	**Auto** On Off	'On' or 'Off' turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric keypad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

I/O Device Configuration sub menu:

Feature	**Option**	**Description**
Local Bus IDE Adapter:	Disabled **Enabled**	Enables onboard IDE device.
Floppy disk controller	Disabled **Enabled** Auto	Enables onboard FDC controller.
Base I/O address	**Primary** Secondary	Selects base address of onboard FDC controller. (Primary = 3F0h, Secondary = 370)
Serial port A Serial port B	Disabled **Enabled** Auto OS Controlled	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port. OS Controlled lets the PNP OS configure the port after bootup.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port A and B.
IRQ	IRQ 3, IRQ 4, IRQ 10 (only port A), IRQ 11 (only port B)	Select IRQ of port A and B.
Serial port C Serial port D	**Disabled** Enabled	Disabled turns off the port. Enabled sets port C to IRQ 4, address 3f8h and port D to IRQ3, address 2f8.
Parallel Port	Disabled Enabled **Auto** OS Controlled	'Disabled' turns off the port. 'Enabled' requires end user to enter the base I/O address and the IRQ. 'Auto' makes the BIOS configure the port. 'OS Controlled' lets the PNP OS configure the port after bootup.
Mode	Output only **Bi-directional** ECP EPP	Set the mode for the parallel port.
Base I/O address	378h, 278h, 3BCh	Select I/O base of port.
IRQ	IRQ 5, IRQ 7	Select IRQ of parallel port.
DMA	DMA 1, 3	Select DMA channel of port if in ECP mode.
‣ Watchdog Settings	sub menu	Opens Watchdog Settings sub menu
Onboard CAN controller:	Disabled **Enabled** Auto OS Controlled	'Disabled' turns off the onboard CAN controller. 'Enabled' requires end user to enter the base I/O address and the IRQ. 'Auto' makes the BIOS configure the controller. 'OS Controlled' lets the PNP OS configure the controller after bootup.

Base I/O address	400, 1000, 1600, **2000**	Set the base I/O address of the onboard CAN controller (range = 256 Byte).
IRQ	**5**, 9	Select the interrupt for the onboard CAN controller.
Onboard Ethernet controller:	Disabled **Enabled**	Enable /disable the onboard PCI Ethernet controller.

Watchdog Settings sub menu:

Feature	**Option**	**Description**
Mode	**Disabled** Reset NMI	Select watchdog operation mode.
Delay	No Delay 0.5s, 1s, **2s**, 4s, 8s, 16s, 32s	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	0.5s, 1s, 2s, **4s**, 8s, 16s, 32s	Max. trigger period.

19.1.3 The Security Menu

Selecting „Security“ from the menu bar displays this menu:

Feature	**Option**	**Description**
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Password on boot	**Disabled** Enabled	‘Enabled’ requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is ‘Disabled’, BIOS assumes user is booting.
Diskette access	User **Supervisor**	‘Enabled’ requires supervisor password to access floppy disk.
Virus check reminder	**Disabled**	Displays a message during bootup asking

System backup reminder	Daily Weekly Monthly	whether you backed up the system or scanned for viruses (Y/N). Message returns on each boot until you respond with "Y". 'Daily' displays the message on the first boot of the day, 'Weekly' on the first boot after Sunday, and 'Monthly' on the first boot of the month.

Enabling "Supervisor Password" requires a password for entering Setup.
The passwords are **not case sensitive**.

Please Note: User and Supervisor passwords are related. You cannot have a User password without first creating a Supervisor password.

19.1.4 The Boot Menu

See chapter "Boot Utilities" below

19.1.5 The Exit Menu

The following sections describe the five possible options of the Exit Menu. Note that <Esc> does not exit this menu. You must select one of these items from the menu to exit.

- Exit Saving Changes

Saves all the selections and exits setup. The next time you boot, BIOS will configure the system according to the Setup selection stored in CMOS.

- Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

- Load Setup Defaults

Select to display the default values for all the Setup menus.

- Discard Changes

If during a Setup session you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

- Save Changes

Saves all the selections without exiting Setup. You can return to the other menus to review and change your selections.

19.2 Boot Utilities

19.2.1 QuietBoot

Right after you turn on or reset the computer, Quietboot displays a graphical logo instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:
- You press <Esc> to display the POST screen
- You press <F2> to enter Setup
- POST issues an error message
- The BIOS or an option ROM requests keyboard input

19.2.2 MultiBoot

MultiBoot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CD-ROM or network card. You can select your boot device in Setup, or you can choose a different device each time you boot by selecting your boot device in **The Boot First Menu**.

MultiBoot consists of 6 menus:

- The Setup Boot Menu

Feature	**Option**	**Description**
Floppy Check	**Disabled** Enabled	'Enabled' verifies floppy type on boot; 'Disabled' speeds boot.
Summary Screen	**Disabled** Enabled	If 'Enabled', a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Dark Boot	**Disabled** Enabled	If 'Enabled', system comes up with a blank screen instead of the diagnostic screen during bootup.
‣ Boot Device Priority	Sub menu	Opens boot device priority sub menu
Onboard LAN RPL ROM	**Disabled**	'Enables' Remote Program Load ROM of

	Enabled	the onboard LAN controller. Supports Intel PXE. For more information, see: www.support.intel.com/support/desktopmgmt/pxepdk.htm

- The Boot Device Priority Menu

This menu allows you to select the order of the devices from which BIOS attempts to boot the OS. If BIOS is unsuccessful at booting from one device, during POST it will try the next one on the list.
The items on this menu each may represent the first of a class of items. For example, if you have more than one hard disk drive, Hard Drive represents the first of such drives as specified in the Hard Drive menu described below.
To change the order, select the device you want to change and press <-> to decrease or <+> to increase priority.

Feature	**Option**	**Description**
‣ Removable Devices	Boot priority & sub menu	Sets boot priority of Removable Devices as described in the respective sub menu.
‣ Hard Drives	Boot priority & sub menu	Sets boot priority of Hard Disks as described in the respective sub menu.
ATAPI CD-ROM Drive	Boot priority	Sets boot priority of ATAPI CD: ROM Drives.
‣ Network Boot	Boot priority & sub menu	Sets boot priority of Network Adapters as described in the respective sub menu.

- The Removable Devices Menu

If you have more than one Removable Media drive, select Removable Devices and press <Enter> to display the Removable Media menu and choose which drive is represented in boot-order menu. Note: The standard 1.44MB floppy drive is referenced as “Legacy Floppy Drives”.

- The Hard Drive Priority Menu

If you have more than one bootable hard drive, select Hard Drive and press <Enter> to display the Fixed Disk Menu and choose the boot priority.

- The Network Boot Priority Menu

If you have more than one bootable network adapter in the system, select Network Boot and press <Enter> to display the available network adapters and choose the boot priority.

- The Boot First Menu

Display the Boot First Menu by pressing <Esc> during POST. In response, the BIOS first displays the message "Entering Boot Menu..." and then displays the Boot Menu at the end of POST.

Use the menu to select any of these options:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, BIOS reverts to the previous boot sequence.
- Enter Setup
- Press <Esc> to continue with the existing boot sequence.

19.3 BIOS Update with Phoenix Phlash

Phoenix Phlash gives you the ability to update your BIOS from a floppy disk without having to install a new ROM chip. Phoenix Phlash is a utility for 'flashing' a BIOS to the Flash ROM installed on the ***MOPS/520***.

Use Phoenix Phlash for the following tasks only:
- Update the current BIOS with a newer version
- Restore a BIOS when it has become corrupted (see below)

Phoenix Plash can be downloaded as a compressed file CRISP489.ZIP from the JUMPtec® web page and contains the following files:

MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette
CRISBOOT.BIN	The Crisis Recovery boot sector code
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode
PHLASH.EXE	Programs the flash ROM
WINCRISIS.EXE	Executable file for creating the Crisis Recovery Diskette from Windows
WINCRISIS.HLP	The help file of WINCRISES.EXE
PLATFORM.BIN	Performs platform-dependent functions
BIOS.ROM	Actual BIOS image to be programmed into flash ROM

To install Phoenix Phlash on your hard disk, unzip the content of CRISP489.ZIP into a local directory, presumable C:\PHLASH.

To create the Crisis Recovery Diskette insert a clean diskette into drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette:

MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode
PHLASH.EXE	Programs the flash ROM
PLATFORM.BIN	Performs platform-dependent functions
BIOS.ROM	Actual BIOS image to be programmed into flash ROM

If the BIOS image (BIOS.ROM) changes due to an update or bug fix, you can easily update the Crisis Recovery Disk. Simply copy the new BIOS.ROM image onto the diskette.

You can run Phoenix Phlash in one of two modes:

- Command Line Mode
- Crisis Recovery Mode

Use the Command Line mode to update or replace your current BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type PHLASH. Phoenix Phlash will automatically update the BIOS. Phlash may fail if your system is using memory managers, in which case the utility will display the following message:

> Cannot flash when memory manager is present.

If you see this message after you execute Phlash, you must disable the memory manager on your system.

19.4 Boot Block Support

Updating the BIOS may create a possible hazard: power failures or fluctuations that occur during the Flash ROM update can damage the BIOS code, making the system unbootable.

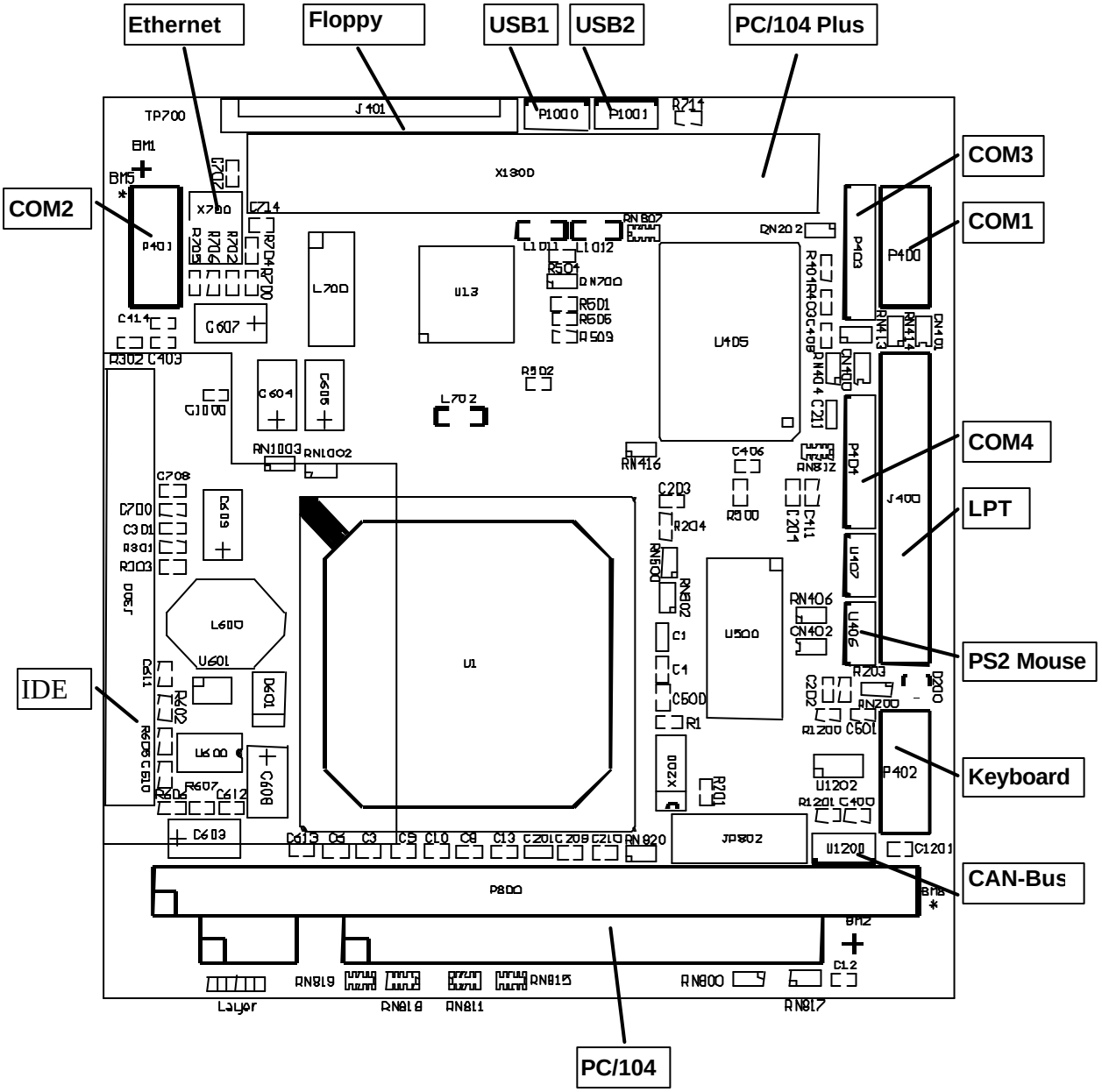
To prevent this possible hazard, the ***MOPS/520*** is equipped with a boot block Flash ROM. The boot block region contains a fail-safe recovery routine. If the boot block code finds a corrupted BIOS (checksum fails), it will boot into the crisis recovery mode and load a BIOS image from a special crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port to force initiating the boot block recovery routine.

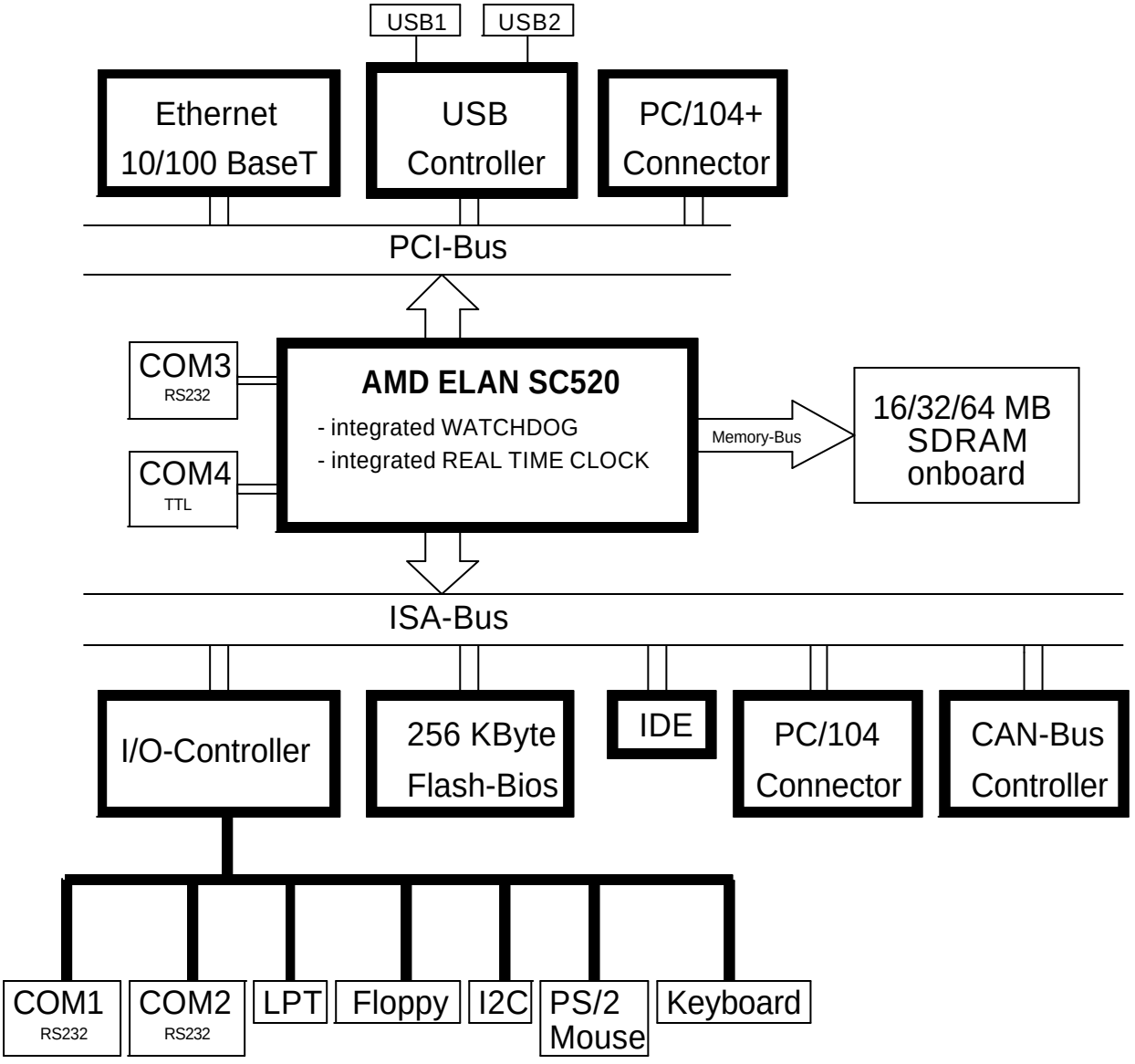
For further information on the update key and the crisis diskette, please visit the JUMPtec® web page.

20. APPENDIX C: CONNECTORS

20.1 Connector Layout



21. APPENDIX D: BLOCK DIAGRAM



22. APPENDIX E: LIMITATIONS

22.1 Parallel Port

Due to certain chipset limitations, parallel port mode ECP, as well as parallel port base address 3BCh (in any mode), cannot be used when a PCI video adapter is installed on the system.

With ISA video adapters these restrictions do not apply.

22.2 Serial Ports

The SC520 integrated serial ports (serial port C and D on the MOPS/520) show two deviations from the standard UART behavior:

The delta ring indicator bit in the modem status register (bit 2) is only set when the ring indicator signal has changed from an ‘active’ to ‘inactive’ state since the last time the modem status register was read. Respectively, this bit is set for RI changes from ‘inactive’ to ‘active’.

In 16550 compatible mode, a received data interrupt is generated when the very first data byte of a continuous data stream is placed in FIFO. This error only occurs for the first character of a continuous data stream received by the UART. Following the FIFO time-out interrupt for the first character received, the remainder of the data stream will be indicated according to the trigger value set in the RFRT bits of the UART FIFO control registers.

22.3 I/O Address Mapping

Only I/O addresses below 400h are mapped to the external ISA bus. All higher I/O addresses are directed to PCI.

22.4 System Clock Deviation

In PC/AT compatible systems, system boot code usually programs the Programmable Interval Timer Channel 0 Count (PIT0CNT) register (port 0040h) to a value of FFFFh. If the timer is based on the PC/AT standard clock of 1.19318 MHz, this results in a periodic IRQ0 generation every 54.93 ms, which is used to keep accurate time of day.
However, as the internal timer clock source of the SC520 is only 1.1892 MHz, setting the standard counter value results in a slower IRQ0 generation rate and inaccurate time of day.

The MOPS/520 BIOS takes care of the deviating clock rate of the SC520 by setting the PIT0CNT to a value of FF25h. However, this only guarantees an accurate system clock for operating systems like DOS, which do not change the value set by the BIOS. If an operating system (like e.g. Windows® 98) re-initializes the PIT0CNT with the standard PC value of FFFFh, it will result in significant system clock deviation.
To solve this problem, set the PIT0CNT to the MOPS/520 value of FF25h again after the operating system has been started.

22.5 Windows â 2000 Support

Windows® 2000 (at least an unmodified standard version) does not run on systems with ISA IDE controllers. During installation or start of a pre-installed system, Windows fails displaying the error message INACCESSIBLE_BOOT_DEVICE. As the MOPS/520 uses an ISA IDE interface, at least a standard Windows® 2000 version cannot be installed or run on the MOPS/520.

22.6 ISA SCSI Support

Due to limitations concerning 16Bit DMA transfers in conjunction with the asynchronous ISA bus timing most ISA SCSI cards can not be used with the MOPS/520.

22.7 Video Support

ISA Graphic Adapters depending on additional ports above 0400h for some special initialization cannot be used with the MOPS/520.

22.8 Watchdog NMI Handling

Although set to NMI mode, the SC520 watchdog will only generate a NMI for the first watchdog timeout. The next time the watchdog timer expires a reset will be generated. To avoid this, the watchdog NMI interrupt service routine must clear bit 12 of the SC520 Watchdog Timer Control register by writing a 1 to this bit. The key sequence 3333h followed by CCCCh must be sent to the register (which is memory mapped to address E400:0CB0) before it can be write accessed. The following code sequence is meant to illustrate the described procedure:

```
.
.
unsigned int wdstore;
volatile unsigned int far *WDTMCTRL;
WDTMCTRL = ((void far *) 0xE4000CB0;
.
.
void interrupt NmiIsr (void)
{
        wdstore = *WDTMCTRL;
        *WDTMCTRL = 0x3333;
        *WDTMCTRL = 0xCCCC;
        wdstore = wdstore | 0x1000;
        *WDTMCTRL = wdstore
}
```

23. APPENDIX F: LITERATURE, STANDARDS, LINKS

For your convenience, JUMP*tec*®has provided the following list of resources regarding standard PC technology.

23.1 PC/104-Bus

- *PC/104 Specification Version 2.3* June 1996, PC/104 Consortium; **www.pc104.org**
- *PC/104-Plus Specification Version 1.1* June 1997
- *PC/104 Consortium;* www.pc104.org
- *Embedded PCs*, Markt & Technik GmbH, ISBN 3-8272-5314-4 (German)

23.2 ISA-BUS, Standard PS/2 Connectors

- *ISA System Architecture*, Addison-Wesley Publishing Company, ISBN 0-201-40996-8
- *AT BUS Design IEEE P996 Compatible*, Edward Solari, Annabooks San Diego CA. ISBN 0-929392-08-6 www.annabooks.com
- *PC Handbook*, Sixth Edition, John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1, www.annabooks.com
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA Bus Specifications and Application Notes, January 30, 1990, Intel
- *Technical Reference Guide*, Extended Industry Standard Architecture Expansion Bus, Compaq 1989
- *Personal Computer Bus Standard P996*, Draft D2.00, January 18, 1990, IEEE Inc.
- *Embedded PCs*, Markt & Technik GmbH, ISBN 3-8272-5314-4 (German)

23.3 PCI Specifications

PCI Special Interest Group, c/o Intel Corporation

PCI System Architecture, Addison-Wesley Publishing Company, ISBN 0-201-40993-3

23.4 RS232C

EIA-232-E Interface between data terminal equipment and data circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)

National Semiconductor's *Interface Data* Book includes several applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering “232” as search criteria shows you a current list of related application notes.

23.5 USB

USB Implementers Forum, Inc., www.usb.org

24. APPENDIX G: CONTACT INFORMATION

24.1 Europe

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Fax: +49 (0) 991-37024-104
URL: www.jumptec.de

24.2 North and South America

JUMP*tec*® Adastra
3988 Trust Way
Hayward, CA. 94545
Tel: 510-732-6900
Fax: 510-732-7655
E-mail: techsupport@adastra.com
URL: www.adastra.com

24.3 Asia

JUMP*tec*® Industrial Computers Asia
5F-1, 341, Sec 4
Chung Hsiao E. Rd.
Taipei, Taiwan
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Fax: +886 2 2772 0314
URL: www.jumptec.com.tw

25. APPENDIX H: DOCUMENT REVISION HISTORY

VERSION	DATE	CHANGES
1.0	09 Aug 01	Created preliminary
1.1	25 Aug 01	Removed preliminary; updated BIOS description; added limitations
1.2	26 Aug 01	Added SCSI and Video limitations
1.3	24 Sep 01	Reformatted
1.4	26 Sep 01	Added drawing in chapter 3.2 Added advanced temperature of D601 in Section 3.4 Added note about the external powerlines (Done by KFR)
1.5	28 Sep 01	Fixed URL syntax on contact page Changed Introduction (Section 2.1) Deleted PCI Slot Table (Section 18.5)