LV2 Main Battery (BAT), Component Design (Includes APS board components)

Version 0.7, Last Modified 7/12/2004

Parts Selection

Throughout what follows, some assumptions are made concerning the umbilical voltage range, umbilical maximum current, battery maximum charge current, etc. Most of these assumptions are store in this variable

```
asu (* assumptions *) =
  {uvmin → 17.75, uvnom → 18, uvmax → 20, uimax → 5,
   vbatmax → 4.2 * 4,
   vbatcutoff → 3 * 4, vbatmin → 2.5 * 4, ibatmax → 4,
   isysmax → 3,
   fmin → 255*^3, fnom → 300*^3, fmax → 345*^3};
```

Issues

Should Q2000 be a dual or single transistor?

What values should be used for output shunt and delay elements? (This amounts to defining load characteristics.)

How will the 4−wireCAN bus be powered?

Is the EMI layout correct? Are the ferrite chokes in the right place?

Connectors (always connectors)

Battery Board (BAT) (100)

Connector(s)

■ CF1
Switch Craft 712A

Umbilical connector on rocket. 5A max.

■ CN100
Phoenix 2.54mm "Euroblock" screw terminals, 4 contact

For the record, these connectors are too big and very inconvenient to use, requiring much time and access to get wires in and out. They are rated 6A per leg, which is nice.

■ CN101
??? Not yet selected

We are considering a high density PCB connector on a daughter board to make the transition to flexible cable. The reverse would occur on the APS board.

Integrated Circuit(s)

■ U100
LTC4150IMS (industrial temp. range), MSOP−8

Battery charge counter.

The LTC4150 is an integrated bipolar voltage to frequency converter designed for monitoring battery charge.

■ U101
MAX399EEE (industrial temp. range), QSOP−16

Analog multiplexer for individual cell voltage measurement.

Capacitors(s)

■ C100
4.7μF 25V 1206

Filter capacitor for battery current shunt.

The impedance is on order 4k, the manufacturer recommends 4.7μF

$$\frac{1}{2\pi R C} /. \{R \to 4*^3, C \to 4.7*^-6\} \ (* \text{ Hz } *)$$

```
8.46569
```

The break frequency is only 8.5Hz! Well, hopefully, fast spikes average to zero.

We'll assume the manufacturer knows what it's talking about and stick with 4.7μF. The leakage on the capacitor should be $\lesssim$10nA . This is within the range of ceramic capacitors. Typically the leakage on ceramic caps isn't given. However, may instruments have a 10MΩ impedance, and 10nA across 10MΩ produces 100mV, which is easily detectable, so if pressed we can measure the leakage.

■ C101
4.7μF 25V 1206

Supply bypass capacitor for battery current counter (U100)

Manufacturer recommends 4.7μF. Since we are using this value already, this is fine.

■ C102
0.1μF 50V 1206

Bypass capacitor for U101, battery voltage multiplexer.

The mux is powered through a 2k impedance (See R102, R103). Because of this a bypass capacitor provides local energy for possible fast transitions. It also makes the designer feel better. The value chosen is one on hand. A 25V rating would work, 50V is more fun.

Resistors(s)

■ R100
P10MCT−ND,10mΩ 1W 2512 (Panasonic ERJ−M1WSF10MU)8.16$/10

50mV shunt for battery charge counting.

The best thing in the DigiKey catalog are the Panasonic SMT thick film resistors. At 5A the dissipation is 1/4W, so a 1/2W resistor is a possibility but the 1/2W packages are ±300ppm/°C for the lower values. The 1W package is ±100ppm/°C for 10mΩ . Maybe 1W is better anyway.

■ R101
1M 5% 1206

Passive shutdown for battery charge counter.

When the battery is disconnected, R101 pulls down the SHDN\ line on U100. Arguable a 100k could be used here, but a 1M is sufficient since maximum input currents for CMOS is typically ~100nA and 100nA across 1M is only 100mV.

■ R102, R103
1k 5% 1206

Avalanche current limiting resistors.

The analog mux U101 is running too close to it's rated voltage (operating voltage 16.8V, rated 17V). So some voltage breakdown is possible during transients. Fortunately the supply current is only 1μA on each leg, so voltage drop is not a serious problem.

The no−latch−upcurrent rating is 30mA, assume 100% over voltage

```
17 / 30*^-3 (* Ohms *) // N // EngineeringForm
```

```
566.667
```

Voltage drop

```
% * 1*^-6 // EngineeringForm (* Volts *)
```

$$566.667 \times 10^{-6}$$

Going to 1k will raise the drop to 1mV. This doesn't seem at all serious.

■ R104
1M 5% 1206

Passive shutdown for battery voltage analog multiplexer.

See R101.

■ R105
20.0k 1% 1206

Bottom end of battery voltage divider.

R105 together with R106 form a resistive voltage divider to scale the maximum battery voltage into the 0−5V range usable by the PIC's A/D.

Initially, scaling 0−20V→ 0−5V seems desirable, but 20V is close to 20.48V, and scaling 20.48V to 5V results in even 20mV quanta, which if easy, is convenient.

Find the required resistance ratio

```
R106/R105 /. Solve[5/20.48 == R105/(R105 + R106), R106][[1]]
```

```
3.096
```

In standard values 61.9k / 20.0k works well. The Thevenin impedance is

```
A B/(A + B) /. {A → 61.9*^3, B → 20*^3} // N // EngineeringForm
```

```
15.116 × 10^3
```

Which is close enough.

20V across 62k limits the input current to

```
20 / 61.9*^3 // EngineeringForm (* amps *)
```

```
323.102 × 10^-6
```

Seems great.

■ R106
61.9k 1% 1206

Top end of battery voltage divider. See R105.

■ R107, R108
1k 5% 1206

Charge counter paranoia resistors.

These resistors limit fault currents from the battery into the PIC to non−damaginglevels.

The top voltage present is about 20V. The PIC can withstand about 20mA into a pin. The raw calculation implies a 1k resistor. Assuming 100pF of stray capacitance (certainly too high) a 4.7k gives a time constant of

```
100*^−12 * 4.7*^3 (* seconds *) // EngineeringForm
```

$470. \times 10^{-9}$

This is actually a bit of an issue, the INT\ pulse width is 1μs minimum. It is prudent to keep the pulse edges crisp compared to the pulse width, so a 1k sounds safer.

■ R109, R110, R111, R112
4.7k 5% 1206

Paranoia resistors for battery board to PIC interface.

Unlike R107, R108, the need for speed on these lines is minimal, so for extra protection, raise the value to 4.7k (See also R107, R108).

Miscellaneous

■ B100

Panasonic_LiIon_Precautions.pdf,April 2002, recommends storing after charging to 50% of capacity, and charging once per year to prevent over−discharge.

■ RT100
2322−640−66103ÞC1482−ND0.61$ Radial Lead

Battery thermistor.

The ’4007 hopes for a thermistor with a Low / High temperature resistance ratio of 7:1 . If this is the case, R2010 = RT100[Max]. The manifest voltage thresholds are

```
Vcold → Vprobe / 2;
```

```
Vhot → Vprobe / 8;
```

The data sheet gives Vprobe = 4.5V nominal, Vcold ±4%, Vhot±8%.

The prospective unit has R[25°C] = 10kΩ±3% , β[25C, 85C] = 3977K±0.075% (datasheet: 23226403.pdf)

The manufacturer of our batteries stupidly does not indicate an allowable temperature range for charging on their datasheet. We will assume the range 0°C to 45°C, which is something of an industry standard for Li+ batteries. (See for example Panasonic_LiIon_Charging.pdf, April 2002 .) (BTW, discharge temperatures should be between −20°C and +60°C, with special precautions below −10°C,see Panasonic_LiIon_Precautions.pdf, April 2002 .)

Using the datasheet values, we can find the ratio of resistance values at the limit temperatures.

```
rteq = Exp[β (1/T - 1/T0)];
```

```
c2f = 273.15 ; (* convert Celsius to Kelvin *)
```

```
(* Assumptions about temperature *)
tempasu = {T0 → 25 + c2f, R0 → 10*^3,
   β → 3977, TLow → 0 + c2f, THigh → 45 + c2f};
```

```
(* low temp resistance *)
r0val = (rteq /. T → TLow /. tempasu )(* ratio — dimensionless *)
```

```
3.39004
```

```
(* high temp resistance *)
r45val = (rteq /. T → THigh /. tempasu)
 (* ratio — dimensionless *)
```

```
0.432345
```

```
r0val / r45val (* Low/High resistance ratio *)
```

```
7.84105
```

This is moderately close to the 7:1 ratio that the ’4007 requires for the simplified thermistor circuit. (See the ’4007 datasheet p.17 .) Try this, leave the high temperature charging cutoff at 45°C, and move the low temperature cutoff up to a 7:1 ratio. If this out below 5°C, then all is well, and we’ll just use the simple circuit. (Though in any case we should layout for the extra resistor required for the more complex circuit, just in case.)

```
Teq = β T0 / (β + T0 Log[r]);
```

```
(Tlowset = (Teq /. r → r45val * 7 /. tempasu) (* degK *))
 - c2f (* display in degC *)
```

```
2.14535
```

2°C is no problem, so use the simplified circuit.

Calculate the thermistor resistance at the low temperature set point

```
Rlowset = (R0 * rteq /. T → Tlowset /. tempasu )(* Ohms *)
```

```
30264.2
```

The closest standard value is 30.1k . The nominal trip points are

```
(* cold trip *)
Teq - c2f /. r → 30.1*^3 / R0 /. tempasu (* degC *)
```

```
2.24904
```

```
(* hot trip *)
Teq - c2f /. r → 30.1*^3 / 7 / R0 /. tempasu (* degC *)
```

```
45.1385
```

Seems alright.

■ F100a, F100b Bussmann SFT−10.0A,10A, proprietary package(SMB??) (DigiKey 283−2439−1−ND1.53$)

Battery fuse..

The main purpose of this device is to prevent the battery pack from exploding in the event of a catastrophic short circuit.

The nominal pack capacity is 4A·Hr, figuring a maximum draw of 10C or 40A, we settled on a 40A fusible link. It's important that the fusing current be rather high because if this link blows we have no power at all.

The internet told me that fuse current of a wire ∝ D^1.5, 12Gage copper (0.0808" Dia) fuses @ 235A, so k = 10232. (16Gage Al melts at 87A) This means a 40A copper fusible link has a diameter of

```
Solve[40 == 10232 Dia^1.5, Dia][[1, 1]] (* Inches *)
```

```
Dia → 0.0248161
```

24ga has nominal dia. 20.1/1000", 22ga is 25.3/1000"

```
10232 #^1.5 & /@ {0.0201, 0.0253} (* amps *)
```

```
{29.1578, 41.1757}
```

So according to this, 24ga is severely oversize but 22ga is about right.

The current density at the fuse point in 22ga is about

```
%[[2]] / (π (0.0253 * 25.5 / 2)^2) (* amps/mm^2 *)
```

```
125.959
```

In inductor coils 4A/mm^2 is conservative. What is a decent figure in PCB's? Linear Tech's an53.pdf sez 50A per inch width of 1oz copper is conservative. Figuring 10z copper as 0.0343mm thick, this is a current density of

```
50 / (25.4 * 0.0343) (* amps/mm^2 *)
```

```
57.3908
```

Clearly there's a lot going on. Any roll−your−own solution will be problematic.

A search here and there and mostly DigiKey reveals that there are no 40A surface mount fuses. So i suggest this. Use two parallel 10A surface mount fuses. In fact we have no good data to suggest that parallel fuses will share current well, but it seems clear that they will share current some. A 10A fuse is sufficient to run our whole load (about 3A) so it could be argued that parallel fuses serve reliability through redundancy.

The fuses of interest typically withstand 100% overload for about 1 second so at a minimum we can surge to 20A for a short period, which is already pretty high current. If current sharing is good, the ~1s surge will be 40A, which is about what we want. And if one fuse is totally ineffectual we still have 10A fusing with multiplied reliability. This seems ok.

Little fuse has a 1206 10A fuse (Cat# 04660‘0.NR) but its interrupt rating is only 35A which may be less than the batteries capacity. The Bussmann SFT−10.0Ais bigger, but interrupts 300A, which is more like it.

Avionics Power System (APS) (2000)

Connector(s)

- **CN2000**
  Phoenix 2.54mm "Euroblock" screw terminals, 4 contact

- **CN2001**
  Phoenix 2.54mm "Euroblock" screw terminals, 4 contact

- **CN2002, CN2003, CN2004, CN2005**
  Phoenix 2.54mm "Euroblock" screw terminals, 4 contact

Integrated Circuit(s)

- **U2000**
  LTC4007EGN, SSOP−24

Internally the chip fixes several parameters

```
fixed = {Vref → 1.19, Vflag → 0.397, iprobe → 11.67*^-6};
```

Datasheet 4007f.pdf, diagram p.8 is not very clear. Using LV2 numbering, this is how it works. The battery voltage is sampled by pulling 11.67μA through R2005. The voltage at the BAT pin is therefore

```
Vbat - R2005 * iprobe /. fixed /. R2005 → 3.01*^3 // EngineeringForm
```

$$-35.1267 \times 10^{-3} + \text{Vbat}$$

This is assuming the recommended value of 3.01k for R2005. The 35mV drop is added back before the battery voltage is applied to the mux. The 35mV drop is not too large to greatly effect the accuracy.

```
100 * 35*^-3 / 14.4 (* (%) of battery voltage *)
```

```
0.243056
```

The internal thresholds for the demuxed voltage are

0.708V −−lowbat, 1.105V −−charger restart, 1.19V −−max cell voltage, 1.28V −−overvoltage protection

In our case (4 x 4.2V), these correspond to per−cellvoltages of

```
{0.708, 1.105, 1.19, 1.28} 4.2 / 1.19
```

```
{2.49882, 3.9, 4.2, 4.51765}
```

The corresponding voltages for a 4−cellpack are

```
% * 4
```

```
{9.99529, 15.6, 16.8, 18.0706}
```

The charging current is measured by R2003, the high side voltage of R2003 is sampled through R2004. CA1 adjusts the current through R2004 until the voltage at pin CSP equals the voltage at the BAT pin. The net effect of this is that a current proportional to the instantaneous charging current flows out of pin PROG. This current is converted into a voltage by R_PROG (R2007/R2008). C2004 together with R_PROG filters out the fast components of the charging current signal to produce an average value.

Each switching cycle is normally terminated when the I_CMP comparator detects that the instantaneous charging current has reached the threshold value. When bulk charging, the current threshold is set by CA2

The current into the CSP pin is

```
icspeq = (icsp /. (Solve[
       ichg * R2003 - R2004 * icsp == -iprobe * R2005,
       icsp][[1, 1]] // Simplify))
```

$$\frac{\text{ichg}\ \text{R2003} + \text{iprobe}\ \text{R2005}}{\text{R2004}}$$

```
% /. {ichg R2003 → 0.1, iprobe R2005 → 0.035}
```

$$\frac{0.135}{\text{R2004}}$$

If we assume the voltage at PROG is 1.19V during bulk charge then the voltage on the high side of the internal 9k resistor is

```
1.19 + 9*^3 * %
```

$$1.19 + \frac{1215.}{R2004}$$

```
% - 1.19 /. R2004 → 3010
```

```
0.403654
```

So the estimated instantaneous charging current signal across the internal 9k when the charging current is just equal to the intended maximum average charging current is 400mV.

CA2 monitors the average charge current, and adjusts I_th so that the voltage at PROG is 1.19V.

The way this works is the voltage at I_TH (Vith) keeps rising until its value divided by 5 is just large enough above that the resulting Δi current through the inductor, combined with the switch timing, produces an average current equal to that which results in a voltage of 1.19V on the PROG pin.

```
vprogeq = icspeq * rprog
```

$$\frac{(ichg\ R2003 + iprobe\ R2005)\ rprog}{R2004}$$

```
dv9keq = icspeq * 9000 (* voltage across 9 k resistor *)
```

$$\frac{9000\ (ichg\ R2003 + iprobe\ R2005)}{R2004}$$

This is all easy enough, what's missing is the timing issues for the current through the inductor.

During ton the voltage across the inductor is (Vin−Vbat),during toff it is simply (Vbat). The data sheet claims circuitry such that

```
toffru = (toff → (Vin - Vbat)/(Vin * f));
```

Where (1/f = ton + toff)

Since the volt·seconds must balance in steady state

```
ton * (Vin - Vbat) == toff * Vbat /. toffru // FullSimplify;
```

```
Solve[%, ton][[1, 1]]
```

$$\text{ton} \to \frac{\text{Vbat}}{\text{f Vin}}$$

The total Δi in the inductor is simply

```
dieq = (ton * (Vin - Vbat) / L /. % // FullSimplify)
```

$$\frac{\text{Vbat}\,(-\text{Vbat} + \text{Vin})}{\text{f L Vin}}$$

If we assume a value for the average inductor current (iavg), then the peak inductor current is just (iavg + Δi/2)

Assuming that iavg is the current resulting in vref on the PROG pin, the voltage across the 9k (dvdi9k), at a given Δi/2 (call this di2) is

```
Vref == vprogeq /. ichg → iavg (* closed loop vprog value *)
```

$$\text{Vref} == \frac{(\text{iavg R2003} + \text{iprobe R2005})\,\text{rprog}}{\text{R2004}}$$

```
dvdi9k == dv9keq /. ichg → iavg + di2 (* peak voltage across 9 k *)
```

$$\text{dvdi9k} == \frac{9000\,((\text{di2} + \text{iavg})\,\text{R2003} + \text{iprobe R2005})}{\text{R2004}}$$

```
Solve[{%, %%}, dvdi9k, iavg][[1, 1]] // FullSimplify
```

$$\text{dvdi9k} \to \frac{9000\,(\text{di2 R2003 rprog} + \text{R2004 Vref})}{\text{R2004 rprog}}$$

Now, with the differential gain across the 9k and the inductor timing relations it seems we know everything about the linearized behavior of this loop.

To keep the battery from discharging through the inductor, the off−phaseis terminated by the I_REV comparator if the voltage across the 9k falls below 17mV. Assuming recommended values, this occurs when the current reaches

```
Vref == vprogeq /. ichg → iavg
```

$$\text{Vref} == \frac{(\text{iavg}\ \text{R2003} + \text{iprobe}\ \text{R2005})\ \text{rprog}}{\text{R2004}}$$

```
17*^-3 == dv9keq /. ichg → iavg * α
```

$$\frac{17}{1000} == \frac{9000\ (\text{iprobe}\ \text{R2005} + \text{iavg}\ \text{R2003}\ \alpha)}{\text{R2004}}$$

```
Solve[{%, %%}, α, iavg][[1, 1]] // FullSimplify
```

$$\alpha \to \frac{(17\ \text{R2004} - 9000000\ \text{iprobe}\ \text{R2005})\ \text{rprog}}{9000000\ (-\text{iprobe}\ \text{R2005}\ \text{rprog} + \text{R2004}\ \text{Vref})}$$

```
% /. R2005 → R2004 /. rprog → 26.7*^3 /. fixed // FullSimplify
```

$$\alpha \to -0.297305$$

That is −30%of its set maximum average current.

For that matter, the set maximum average charge current in terms of resistor values is

```
iavgmaxeq = (ichg /. Solve[
      Vref == vprogeq,
      ichg][[1]] // FullSimplify)
```

$$\frac{-\text{iprobe}\ \text{R2005}\ \text{rprog} + \text{R2004}\ \text{Vref}}{\text{R2003}\ \text{rprog}}$$

A slightly trickier issue than the set current is the trip point of the nearly charged FLAG\, which occurs at the internally fixed threshold of Vflag=397mV. The corresponding current at this threshold is

```
iflageq = (ichg /. Solve[
      Vflag == vprogeq,
      ichg][[1]] // FullSimplify)
```

$$\frac{-\text{iprobe}\ \text{R2005}\ \text{rprog} + \text{R2004}\ \text{Vflag}}{\text{R2003}\ \text{rprog}}$$

Investigate the recommended value case:

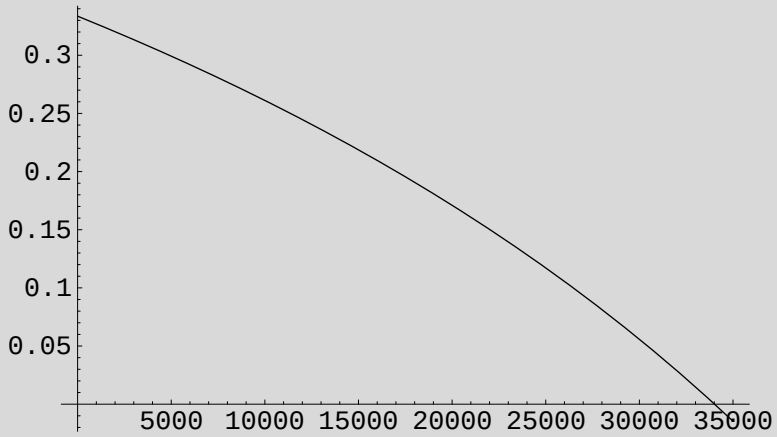
```
iflageq / iavgmaxeq // FullSimplify
```

$$\frac{\text{iprobe R2005 rprog} - \text{R2004 Vflag}}{\text{iprobe R2005 rprog} - \text{R2004 Vref}}$$

```
rncthc = (* Relative Nearly Charged THreshold Current *)
 (% /. fixed /. R2005 → R2004 // FullSimplify)
```

$$1. + \frac{67952.}{-101971. + 1.\ \text{rprog}}$$

```
Plot[%, {rprog, 0, 35*^3}];
```




```
rncthc /. rprog → 26.7*^3
```

```
0.0972335
```

Clearly the value of R_PROG couples to the nearly charged current threshold as well as the peak charge current.

In the data sheet (p.13−14)an example with R2004/R2005 = 2.49k is given.

```
rprogru = Solve[iavgmaxeq == imax, rprog][[1, 1]]
```

$$\text{rprog} \to \frac{\text{R2004 Vref}}{\text{imax R2003} + \text{iprobe R2005}}$$

Well, maybe i don’t need this the rprog rule now, but it’s good to have around anyway. From the example, the max avg charge current is

```
iavgmaxeq /. fixed /. R2005 → R2004 /.
 {rprog → 26.7*^3, R2003 → 0.033, R2004 → 2490}
```

```
2.4824
```

Since R_PROG is unchanged from the nominal case, by the ncthld equation, the nearly charged trip point remains at 10% I_MAX.

The difficult part of the example is in the obscure last paragraph.

"There are other effects to consider.
The voltage across the current comparator is scaled to obtain the same values as the 100mV sense voltage target, but the input referred sense voltage is reduced, causing some careful consideration of the ripple current.
Input referred maximum comparator threshold is 117mV, which is the same ratio of 1.4x the DC target.
Input referred IREV threshold is scaled back to -24mV.
The current at which the switcher starts will be reduced as well so there is some risk of boost activity.
These concerns can be addressed by using a slightly larger inductor to compensate for the reduction of tolerance to ripple current."

Taking these points in order, reducing R2004 increases the current flowing into pin CSP. Therefore there is no difference between the nominal and example case in terms of the voltages of internal comparators and control loops.

The 2nd point mentions "input referred sense voltage". Really have no idea what this means. The only thing that is reduced is the voltage excursion across the sense resistor

```
0.033 * 2.5 // EngineeringForm
```

```
82.5 × 10^-3
```

82.5mV instead of 100mV, so what?

Don’t know where the 117mV came from. Certainly for some combination of conditions 117mV will be the proper trip point. The ratio 1.4 ≃ .117 / 0.0825 is a misunderstanding. The ripple is measured above and below the average current, so the correct 1.4x ratio is actually a trip voltage of 0.0825 * 1.2 = 99mV across the shunt.

The reverse threshold of course also scales. The current at which the switcher starts is unaffected.

Charger Start−Up:
When the charger is enabled, it will not begin switching until the ITH voltage exceeds a threshold that assures initial current will be positive. This threshold is 5% to 15% of the maximum programmed current. After the charger begins switching, the various loops will control the current at a level that is higher or lower than the initial current. The duration of this transient condition depends upon the loop compensation, but is typically less than 100µs

Hmm, ok, think about the inductor/switch timing

During the on time, the applied V·s are

```
ton * (Vin - Vbat)
```

During off

```
-toff * Vbat
```

Also

```
ton + toff == 1 / f
```

The datasheet claims toff is forced to be

```
toff → (Vin - Vbat) / (Vin * f)
```

Therefore the V·s during off are

```
-toff * Vbat /. toff → (Vin - Vbat) / (Vin * f) // Simplify
```

$$\frac{\text{Vbat}\,(\text{Vbat}-\text{Vin})}{\text{f Vin}}$$

Assuming V·s balance

```
% + ton (-Vbat + Vin) == 0 // FullSimplify
```

$$\frac{(\text{Vbat}-\text{Vin})\,(\text{Vbat}-\text{f ton Vin})}{\text{f Vin}} == 0$$

```
Solve[Vbat - f ton Vin == 0, ton][[1, 1]]
```

$$\text{ton} \to \frac{\text{Vbat}}{\text{f Vin}}$$

The average current is 1/2 way between the ΔI

```
Δi → ton * (Vin - Vbat) / L /. %
```

$$\triangle\text{i} \to \frac{\text{Vbat}\,(-\text{Vbat}+\text{Vin})}{\text{f L Vin}}$$

If we target Δi = 0.4 * i_avg (see datasheet p.15)

```
icspeq /. {ichg R2003 → 0.0825 * 1.2, R2005 → R2004}
```

$$\frac{0.099 + \text{iprobe R2004}}{\text{R2004}}$$

```
% /. fixed /. R2004 → 2490 // EngineeringForm
```

$$51.429 \times 10^{-6}$$

```
icspeq /. {ichg R2003 → 0.1 * 1.2, R2005 → R2004}
```

$$\frac{0.12 + \text{iprobe R2004}}{\text{R2004}}$$

```
% /. fixed /. R2004 → 3010 // EngineeringForm
```

$$51.5371 \times 10^{-6}$$

I think this paragraph was not written by the same author as the preceding ones. It contains several errors which seem to stem from the fact that the previous author calculated "input referred" voltages across the shunt and presented those as thresholds for various functions of the IC, when in fact the actual thresholds are taken from the current source controlled by CA1, which has no direct knowledge of shunt voltages at all.

From now on this paragraph will be ignored.

■ U2001 LTC4412ES6, SOT−23−6

Battery power saturating rectifier controller.

U2001 monitors the voltage on the umbilical positive conductor and the battery positive conductor. When the battery voltage is higher it turns on Q2004, which is connected as a diode, thereby eliminating the typical voltage loss across a forward conducting diode.

The LTC4412 uses a linear regulating loop to control the FET, when turned on, the FET is not actually in hard saturation, rather the forward voltage is regulated to 20mV (minimum 10mV). Therefore there is maximum Rdson for a given load current, that will just allow the FET to reach the desired voltage when on. If we assume 5A as the maximum current that resistance is

```
Rdson_Max → Vf / imax /. {Vf → 10*^−3, imax → 5} // N //
 EngineeringForm (* Ohms *)
```

```
Rdson_Max → 2. × 10^−3
```

This value of resistance is difficult to achieve in the year 2004 with a conveniently sized P−FET.A typical candidate is the Vishay Si4429EDY featuring an Rdson of 10.5mΩ at 10V, 25C (8.6mΩ typ.).

At the current system load, the achievable voltage with this part is

```
Rdson * isysmax /. Rdson → 10.5*^−3 /. asu // N // EngineeringForm
```

```
31.5 × 10^−3
```

Which is pretty good. The dissipation is

```
% * isysmax /. asu // EngineeringForm (* Watts *)
```

```
94.5 × 10^−3
```

In the worst case, assuming 40C temperature rise, the dissipation would be

```
i^2 Rdson25 * δT /. {i → 5, Rdson25 → 10.5*^−3, δT → 1.3} (* Watts *)
```

```
0.34125
```

Figuring θ = 80°C/W the implied temperature rise is

```
80 * % (* degC *)
```

```
27.3
```

Which is consistent with the assumptions made. So this part would work.

A pretty reasonable question is what is the maximum allowable Rdson that will still handle the maximum 5A?

Let δ be the relative change in Rdson as the temperature deviates from 25°C

```
Solve[
  Tj == Ta + θ * i^2 Rdson25 * (1 + δ (Tj - T0)),
  Rdson25][[1, 1]]
```

$$\text{Rdson25} \to -\frac{\text{Ta} - \text{Tj}}{\text{i}^2\ (1 - \text{T0}\,\delta + \text{Tj}\,\delta)\,\theta}$$

Assuming a typical so8 transistor

```
% /. {Ta → 60, Tj → 150, i → 5, T0 → 25, δ → 5*^-3, θ → 80} // N //
 EngineeringForm (* Ohms *)
```

$$\text{Rdson25} \to 27.6923 \times 10^{-3}$$

■ U2002, U2003, U2004, U2005
LTC1154CS8, SO−8

Power switches for system loads.

Considered LT1910, very high off current (2.5mA Max). Likewise the LT1161. Considered the LTC1981, which has the right package (SOT−23) but no current limiting, and only 7.5V maximum supply voltage. Considered the IPS511/512 which current limits at a semi convenient 5A, but has an Rdson of 0.15Ohms max and a minimum current limit of 3A. The IPS5451 is similar but goes way too far the other way with a max limit of 50A even though its continuous output current rating is only 4A. (BTW if you want to understand IR's IPS line, read their design tips dt99−4and dt−99−6.)We also checked TI, Vishay, Maxim, SGS, OnSemi (the NIS5102 is an interesting device), Micrel, National, Toshiba, Infineon and the internet and found nothing better than the LTC1154, which is far from ideal. The package is too big (so8) and the single FET driver has too many pins devoted to inputs (3), but it will run at 20V(barely), does current limiting with a somewhat reasonable 100mV±25% shunt (should be 50mV) and it draws too much off current (20μA max). The LTC1153 is almost identical but features automatic reset after a delay programed by an external capacitor.

Since the VGS may approach 25V, a logic level FET probably won't work. A 25V rated part probably will. Also a zener diode could be used (15V probably). A supply filter is recommended to power the switch during short circuits (datasheet Fig.8 p.10).

Transistor(s)

■ Q2000
Si4429EDY, SO−8

Input FET for battery charger. This FET operates as a saturated rectifier. Its main function is to prevent current flow from the rocket into the umbilical.

Currently (v0.5) the schematic still shows two FETs for Q2000. I'm ambivalent. 7A is a lot, but we probably won't see 7A for quite awhile, if ever. Somebody else needs to tip my mind.

The primary selection criterion for this FET is R_DSON. The full umbilical current flows through the FET. Since we may decide to push the umbilical a little bit, we should figure the entire load, system + battery, and see if we can satisfy the dissipation limit using a P−FET.

The maximum gate drive for Q2000 is clamped between 5V and 6.5V, so a logic level FET is recommended.

Flipping the DigiKey catalog suggests the TPC8106−H. The R_DSON is < 24mΩ . Assume thermal resistance of 100C/W

```
imax → ibatmax + isysmax /. asu
```

```
imax → 7
```

```
Pmax → imax^2 rdson /. % /. rdson → 0.024
```

```
Pmax → 1.176
```

Tjmax for this part is 150C, assuming 65C ambient, allowable dissipation is

$$\frac{150 - 65}{100} \,//\, N$$

```
0.85
```

BTW, the ’4007 regulates the forward voltage to 50mV. At 7A, the minimum achievable voltage is 168mV, so the transistor, rather than the chip, is the limiting factor.

A single transistor is marginal for 6A. Two transistors easily handle the full load current. Use two parallel FETs and see if anyone yells.

Nope, changed my mind. Size it for 5A.

```
100 * 5^2 * 0.024 (* Temp. rise [C] *)
```

```
60.
```

This is still plenty hot, and a fair amount of wasted power. Stay with the dual trany.

Since we have the Si4429EDY, we will use it, and skip the dual trany. Even a single TPC8106 (TPC8106−HCT−ND) would work (see U2001) but the ’4429 is a cleaner solution.

■ Q2001 FDS4435, SO−8

P−FETbuck converter main switch.

A reasonable place to start is with dissipation in the ’4007. The allowable junction temperature on the ’4007 is 125C. The estimated thermal resistance is 90°C/W. Figuring max ambient of 60C, the allowable dissipation is

```
125 C - 60 C
------------ // N
  90 C / W
```

```
0.722222 W
```

Half this would be much more prudent. Try to limit dissipation to around 300mW.

The dissipation equation is given in the ’4007 datasheet, the parameter of interest is the total gate charge of both mosfets

```
Pd == Vin (f Q + io) /. {Vin → uvmax, f → fmax, io → 5*^-3} /. asu
  /. Pd → 0.3;
```

```
Solve[%, Q][[1, 1]] // EngineeringForm
```

```
Q → 28.9855 × 10^-9
```

This gate charge is to be calculated assuming 6V of gate swing, and the full Vin on the drain.

The TPC−8106 P−FETs picked for the InFETs have 33nC total gate charge under these circumstances. Not great. The TPC−8109,optimized for higher speed, is better in this regard with 28nC tgc.

The dissipation in the P−FETis given in the data sheet as

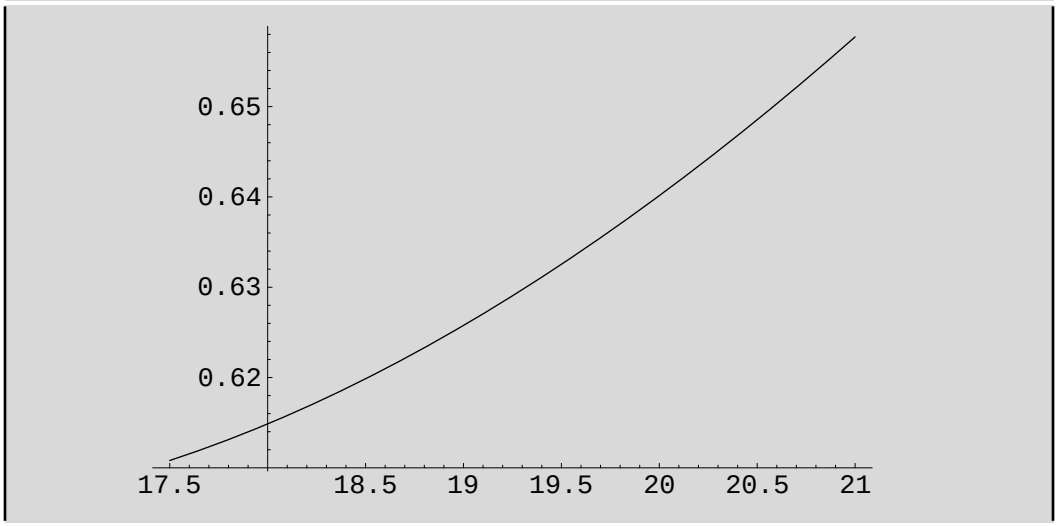
```
Ppfeteq = Vbat/Vin imax^2 (1 + δ T) Rdson + 2 Vin^2 imax Crss f;
```

For the ’8109 the worst case dissipation is

```
Ppfeteq /. {Vbat → vbatmax, imax → ibatmax, f → fmax} /. asu
 /. {Rdson → 0.02, δ → 4.76*^-3, Crss → 290*^-12, T → 40}
```

$$\frac{6.39959}{\text{Vin}} + \frac{2001\,\text{Vin}^2}{2500000}$$

```
Plot[%, {Vin, 17.5, 21}];
```




```
%% /. Vin → 20 (* Watts *)
```

```
0.64014
```

Interestingly, for this case the dissipation is split almost exactly between conduction and drive losses.

The question is, can a P−FETbe found with less total gate charge that still has a reasonable Rdson?

Try:
IR: SI4435DY−ND,so8 30V 0.020 1.50$
IR: IRF7705−ND,TSSOP−830V 0.018 (0.030 @ 4.5V) 1.65$
IR: IRF7424−ND,so8 30V 0.013 (0.022 @ 4.5V) 2.01$ >50°C/W no avalanche rating
Si4431ADY

```
pcandi =


 "Unit"        "Rdson@6V"  "δ"       "Q"       "Crss"    "$"
 "TPC-8109"    0.02        4.76*^-3  28*^-9    290*^-12  1.26
 "SI4435DY"    0.025       3.13*^-3  27*^-9    270*^-12  1.5
 "IRF7705"     0.025       2.5*^-3   35*^-9    270*^-12  1.65
 "IRF7706"     0.028       2.5*^-3   33*^-9    207*^-12  □
 "IRF7726"     0.028       3*^-3     30*^-9    220*^-12  □
 "IRF7424"     0.017       3.9*^-3   48*^-9    410*^-12  2.01
 "SI4431DY"    0.037       4.5*^-3   15*^-9    114*^-12  □
 "IRF7416"     0.025       5*^-3     40*^-9    410*^-12  □
 "IRF7406"     0.06        5*^-3     24*^-9    220*^-12  □
 "NDS9435A"    0.062       3.6*^-3   7*^-9     70*^-12   □
 "NDS8435"     0.035       4.3*^-3   33*^-9    370*^-12  □   ;
 "NDT456P"     0.038       3.75*^-3  34*^-9    355*^-12  □
 "ZXM66P03N8"  0.032       5*^-3     40*^-9    279*^-12  □
 "ZXMP3A16G"   0.055       3.5*^-3   16*^-9    116*^-12  □
 "ZXMP3A16N8"  0.05        3.6*^-3   16*^-9    116*^-12  □
 "FDS4435"     0.025       3.5*^-3   20*^-9    202*^-12  □
 "Si7421DN"    0.03        4*^-3     18*^-9    133*^-12  □
 "Si4435BDY"   0.029       4*^-3     23*^-9    200*^-12  □
 "Si4431BDY"   0.035       4*^-3     16*^-9    190*^-12  □
 "Si9435BDY"   0.055       4.2*^-3   11.5*^-9  116*^-12  □
 "Si6435ADQ"   0.04        5*^-3     19*^-9    166*^-12  □
 "Si4835DY"    0.027       4.5*^-3   22*^-9    220*^-12  □
```

So really, the TPC−8109is about as good as anything. The ’4431 is interesting because it takes the load off the ’4007. The ZXMP3A16C is available as a dual with about the same ratings (ZXM3A16DN8).

```
Ppfetdiseq =
  Ppfeteq /. {Vbat → vbatmax, imax → ibatmax, f → fmax} /. asu;
```

```
Ppfetdiseq /.
 {Rdson → 0.037, δ → 5*^-3, Crss → 114*^-12, T → 40, Vin → 20}
```

```
0.722592
```

```
Vin f Q /. {Vin → uvmax, f → fmax} /. asu /. Q → (28 - 12.5) 1*^-9
```

```
0.10695
```

So going to the ’4431 actually improves overall efficiency. Conduction loss is up about 80mW, but dissipation in the ’4007 drops better than 100mW. This is real good because it would be nice to move dissipation out of the charger chip. A slight problem is that the Si4431 isn’t DigiKey’able. Try another 32mΩ P−FET?

Try IRF7416, IRF7406, NDS9435ACT−ND,NDT456PCT−ND.

Ok, for each candidate P−FET,compute and display the dissipation in the IC, FET, and the total dissipation

```
Picgceq = (Vin f Q /. {Vin → uvmax, f → fmax} /. asu);
(* power in the IC due to gate charge *)
```

```
pfetpwr[rw_] := Module[{Pic, Pfet},
  {rw[[1]], Pic = (N[Picgceq /. Q → rw[[4]]]),
   Pfet = (Ppfetdiseq /. {Vin → 20, T → 40,
       Crss → rw[[5]], δ → rw[[3]], Rdson → rw[[2]]}), Pic + Pfet}
 ]
```

```
pfetpwr /@ Drop[pcandi, 1] // MatrixForm
```

TPC−8109	0.1932	0.64014	0.83334
SI4435DY	0.1863	0.676147	0.862447
IRF7705	0.2415	0.66768	0.90918
IRF7706	0.2277	0.64248	0.87018
IRF7726	0.207	0.664358	0.871358
IRF7424	0.3312	0.716763	1.04796
SI4431DY	0.1035	0.712646	0.816146
IRF7416	0.276	0.85584	1.13184
IRF7406	0.1656	1.21056	1.37616
NDS9435A	0.0483	1.03055	1.07885
NDS8435	0.2277	0.959789	1.18749
NDT456P	0.2346	0.979248	1.21385
ZXM66P03N8	0.276	0.824112	1.10011
ZXMP3A16G	0.1104	0.970752	1.08115
ZXMP3A16N8	0.1104	0.896832	1.00723
FDS4435	0.138	0.606048	0.744048
Si7421DN	0.1242	0.614544	0.738744
Si4435BDY	0.1587	0.672922	0.831622
Si4431BDY	0.1104	0.755424	0.865824
Si9435BDY	0.07935	0.99145	1.0708
Si6435ADQ	0.1311	0.828384	0.959484
Si4835DY	0.1518	0.671078	0.822878

```
Sort[%, (#1[[4]] < #2[[4]]) &] // MatrixForm
```

Si7421DN	0.1242	0.614544	0.738744
FDS4435	0.138	0.606048	0.744048
SI4431DY	0.1035	0.712646	0.816146
Si4835DY	0.1518	0.671078	0.822878
Si4435BDY	0.1587	0.672922	0.831622
TPC−8109	0.1932	0.64014	0.83334
SI4435DY	0.1863	0.676147	0.862447
Si4431BDY	0.1104	0.755424	0.865824
IRF7706	0.2277	0.64248	0.87018
IRF7726	0.207	0.664358	0.871358
IRF7705	0.2415	0.66768	0.90918
Si6435ADQ	0.1311	0.828384	0.959484
ZXMP3A16N8	0.1104	0.896832	1.00723
IRF7424	0.3312	0.716763	1.04796
Si9435BDY	0.07935	0.99145	1.0708
NDS9435A	0.0483	1.03055	1.07885
ZXMP3A16G	0.1104	0.970752	1.08115
ZXM66P03N8	0.276	0.824112	1.10011
IRF7416	0.276	0.85584	1.13184
NDS8435	0.2277	0.959789	1.18749
NDT456P	0.2346	0.979248	1.21385
IRF7406	0.1656	1.21056	1.37616

On the basis of the last matrix, 1st Fairchild FDS4435, 2nd Si4435BDY (scared of obsolescent parts), 3rd Digkey’able TPC−8109.(Currently scared of the Si7421 due to unknown package.)

■ Q2002 TPC8009−H,SO−8

N−FETbuck converter synchronous switch.

Similar to the P−FETQ2001, the gate charge of this FET causes power dissipation in the ’4007. The main difference in terms of power dissipation is that Q2002 switches at low V_DS, so the gate to drain capacitance is not significant.

The data sheet suggests an FDC645N

Try sot−6:,TPC6002, ; tsop8: , IRF7603 ; sot223 IRLL2703, IRLL3303, NDT451,NDT453 ; so8:TPC8009, ∞

```
ncandi = {{"Unit",      "Rdson@6V", "δ",      "Q",       "$"},
          {"FDC645N",   0.029,      3.3*^-3,  17*^-9,    □},
          {"TPC8013-H", 0.0065,     4*^-3,    30*^-9,    □},
          {"NDT453N",   0.035,      7.5*^-4,  20*^-9,    □},
          {"TPC8009-H", 0.011,      4*^-3,    18.5*^-9,  0.81},
          {"NDT451AN",  0.042,      3.8*^-3,  14*^-9,    □},
          {"IRLL3303",  0.039,      5*^-3,    22.5*^-9,  □},
          {"IRLL2703",  0.056,      4*^-3,    11*^-9,    □},
          {"IRF7603",   0.044,      5*^-3,    12*^-9,    □},
          {"TPC6002",   0.029,      5.3*^-3,  9*^-9,     □}};
```

$$\text{Pnfeteq} = \frac{\text{Vin} - \text{Vbat}}{\text{Vin}}\ \text{imax}^2\ (1 + \delta\, T)\ \text{Rdson};$$

```
Pnfetdiseq =
  Pnfeteq /. {Vbat → vbatmin, imax → ibatmax, f → fmax} /. asu;
(* Actually vbatmin & vbatmzx can't occur together! *)
```

```
nfetpwr[rw_] := Module[{Pic, Pfet},
  {rw[[1]], Pic = (N[Picgceq /. Q → rw[[4]]]),
   Pfet = (Pnfetdiseq /.
      {Vin → 20, T → 40, δ → rw[[3]], Rdson → rw[[2]]}), Pic + Pfet}
 ]
```

```
nfetpwr[ncandi[[3]]]
```

```
{TPC8013-H, 0.207, 0.06032, 0.26732}
```

```
nfetpwr /@ Drop[ncandi, 1] // MatrixForm
```

FDC645N	0.1173	0.262624	0.379924
TPC8013-H	0.207	0.06032	0.26732
NDT453N	0.138	0.2884	0.4264
TPC8009-H	0.12765	0.10208	0.22973
NDT451AN	0.0966	0.387072	0.483672
IRLL3303	0.15525	0.3744	0.52965
IRLL2703	0.0759	0.51968	0.59558
IRF7603	0.0828	0.4224	0.5052
TPC6002	0.0621	0.281184	0.343284

```
Sort[%, (#1[[4]] < #2[[4]]) &] // MatrixForm
```

TPC8009−H	0.12765	0.10208	0.22973
TPC8013−H	0.207	0.06032	0.26732
TPC6002	0.0621	0.281184	0.343284
FDC645N	0.1173	0.262624	0.379924
NDT453N	0.138	0.2884	0.4264
NDT451AN	0.0966	0.387072	0.483672
IRF7603	0.0828	0.4224	0.5052
IRLL3303	0.15525	0.3744	0.52965
IRLL2703	0.0759	0.51968	0.59558

■ Q2003
Eliminated v0.5

Originally intended to prevent battery power flowing out through the umbilical, this function is redundant with Q2000.

■ Q2005
ZXMN2A01F, SOT−23−3

Saturated switch controlling trickle charge.

The selected N−FEThas Vdss_max=20V, Rdson=120mΩ @ 4.5V. This is probably more than we need here, but we already have some.

■ Q2006, Q2007, Q2008, Q2009
TPC8013−H,SO−8

Power switches for various loads.

Since we have changed the power controls to high−side drivers + N−FETs, we need N−FETs. These are cheap (0.95$@10) and have decent Rdson (5mΩ), and ok Vgs_max (20V).

Rdson_max @ 10V@25C = 6.5mΩ, Tempco is 4.2E−3,so Rdson_max @100C is

```
6.5*^-3 * (1 + 4.2*^-3 (100 - 25)) (* Ohms *) // EngineeringForm
```

$$8.5475 \times 10^{-3}$$

If we limit to 1/3W dissipation the max DC current is

```
√(1 / 3) / %  (* amps *)

6.24482
```

This seems fine.

Diode(s)

■ D2000
MA2Q705, NMiniP2 (This device is in the PSAS Eagle Library)

Schottky diode, augments synchronous switch Q2002.

A 1A Schottky of sufficient voltage rating (~30V) should be adequate.

On the SPS we use MA2Q705, ’4007 datasheet suggests MBRM140T3.

```
   "Unit"    Vrmax  Imax   Vf    trr
 "MA2Q705"    30    1.5  0.37  50*^-9
"MBRM140T3"   40    1.0  0.36    □

{{Unit, Vrmax, Imax, Vf, trr},
 {MA2Q705, 30, 1.5, 0.37, 1/20000000},
 {MBRM140T3, 40, 1., 0.36, □}}
```

I say use the SPS unit. The MBR is a little smaller, a little less power capable (fine for this application) but the difference is not enough to justify stocking another part.

■ D2001
1N4148WCT−ND,SOD−123(Can also get 1N4448HWS in SOD−323)

Rocket Ready signal diode.

Prior to launch, the umbilical power is disconnected and the umbilical power positive conductor pulled to ground by a 4.7k or greater resistor. Once the FC on the rocket decides that everything is "go" it releases its launch hold by raising the Rocket_Ready (RckRdy) line to ~5V. This signal is conducted by D2001 onto the umbilical power positive conductor. D2001 may be a silicon planer signal diode. A minimum 50V rating is prudent.

We select the 1N4148, since we already use them. The rating on this diode is 75V, SOD−123package.

■ D2002, D2003, D2004, D2005
1N4148WCT−ND,SOD−123(Can also get 1N4448HWS in SOD−323)

Short circuit protection speed up diode.

If the overload delay circuit is used, this diode may be included to bypass the resistor and activate the overload protection when the voltage on the current sensing shunt reaches 700mV (×7 overload). Possibly a Schottky diode could be used here to reduce the short circuit threshold current, but the leakage should be carefully evaluated. See R2036 for details of the overload delay circuit.

■ D2006, D2007, D2008, D2009
1N4148WCT−ND,SOD−123(Can also get 1N4448HWS in SOD−323)

Gate turn off diodes.

If the soft−on delay circuit is used, this diode must be included to bypass the network resistance and accelerate the discharge of the output transistor's gate.

■ Z2000, Z2001, Z2002, Z2003
Diodes Inc. BZT52C15SDICT−ND15V Zener, 3.44/10, SOD−323

Gate protection diodes.

Sadly, many modern, and even semi−modern circuits are designed for low voltages. There is some hope that the situation will improve with the advent of 48V automotive systems but for now working above 12V is often a problem. In this cast the charge pump on the LTC1154, essentially a tripler, does not regulate its output voltage, so at higher supply voltages such as used here there is a possibility that the output transistor's gate may suffer voltage breakdown. These Zener diodes limit the gate voltage to 15V. The extra current drawn from the gate driver is not a problem since it is a high impedance source, and rated for small current drains.

The diodes chosen are 15V units in SOD−323 packages, which are fairly small but shootable, and we already use this package elsewhere.

Inductor(s)

■ L2000a, L2000b
DRQ125−6R8

Buck converter power storage inductor.

From the '4007 datasheet (p.15) the inductor current ripple is

$$\Delta i \to \frac{1}{f\,L}\,Vbat\left(1-\frac{Vbat}{Vi}\right);$$

```
diLmax = (Δi /. % /. {f → fmin, Vi → uvmax, Vbat → vbatmin} /. asu)
```

$$\frac{0.0000196078}{L}$$

The maximum Volt*seconds applied to the inductor is just diLmax * L or 19.6V·μs .

Target Δi max as 0.4 * iavg max

```
Solve[diLmax == 0.4 * ibatmax /. asu, L][[1, 1]] // EngineeringForm
```

$$L \to 12.2549 \times 10^{-6}$$

Meaning that 12μH is a workable value. A hair more would be a hair better.

The inductor must not saturate carrying peak current. This means at least the DC value + Δimax/2. Also the core and copper losses must be reasonable. Industry standards estimate reasonable losses to be such that produce a 40°C temperature rise in the inductor. Typically this works out to losses of about $100\,\mathrm{mW}/\mathrm{cm}^3$ of core volume.

Just 'cuz, here is the RMS value of a triangle wave with DC offset

```
(∫_0^ton (t/ton (imax - imin) + imin)^2 dt +
   ∫_0^toff ((toff - t)/toff (imax - imin) + imin)^2 dt) /
  (ton + toff) // FullSimplify
```

$$\frac{1}{3}\left(\mathrm{imax}^2 + \mathrm{imax}\,\mathrm{imin} + \mathrm{imin}^2\right)$$

```
irms → √% /. {imax → iavg + Δi/2, imin → iavg - Δi/2} //
 FullSimplify
```

$$\mathrm{irms} \to \sqrt{\mathrm{iavg}^2 + \frac{\triangle \mathrm{i}^2}{12}}$$

Hmm, i guess DC terms will always hit the bound.

Hunted and pecked quite a bit, couldn't find a decent inductor. So have decided to use whatever combination of coiltronics DRQ series will work. The DRQ125's are close but a bit too small so will use two in series. Here are the specs (from <DRQ_Specs.pdf> PM−43154/04)

```
                "PN"   "L0"  "Irms"  "Isat"  "Vs"
               "6R8"  6.588   6.64    8.68   12.0
DRQ125 = Drop["8R2"  8.048   5.54    7.86   13.3, 1];
               "100"  9.654   5.35    7.17   14.6
               "150"  15.35   4.27    5.69   18.4
```

Lower inductance values are excluded because of excessive current ripple. Larger values are excluded because of insufficient Irms current.

Compute the V·s fraction

```
(diLmax * L / 2) / (DRQ125[[All, 5]] * 1*^-6)
```

```
{0.816993, 0.737137, 0.671501, 0.532822}
```

Use the "Irms Derating with Core Loss" graph to estimate the allowable Irms loss @ 300kHz

```
allowIrmsloss = {0.71, 0.77, 0.81, 0.88};
```

Using the allowable Irms loss we can find the acceptable rms current.

```
DRQ125[[All, 3]] * allowIrmsloss
```

```
{4.7144, 4.2658, 4.3335, 3.7576}
```

So 15μH doesn't work.

The actual RMS current depends somewhat on the inductance. Using initial inductances

```
(diLmax * L) / (2 * DRQ125[[All, 3]] * 1*^-6) (* amps *)
```

```
{1.47649, 1.76966, 1.83251, 2.296}
```

```
aproxIrms = Sqrt[16 + %^2 / 12]
```

```
{4.02264, 4.03249, 4.03483, 4.05454}
```

These are negligible differences.

The total power loss for each inductor combination can be expressed as a fraction of the +40°C loss.

```
1 - allowIrmsloss (* core loss fraction *)
 + (aproxIrms / DRQ125[[All, 3]])^2 (* actual Irms loss fraction *)
```

```
{0.657018, 0.759818, 0.758778, 1.02163}
```

This result indicates that the 6.8μH inductors are the least lossy even though they have the greatest core loss.

Check the 6.8μH inductors for reasonableness.

The minimum inductance at 20C is

```
L → (2 * 6.8*^-6) * 0.8 // EngineeringForm
```

```
L → 10.88 × 10^-6
```

Don't expect too much inductance loss at cold temperature, none at high temperature.

At peak current the fraction of Isat is

```
(diLmax / 2 + 4) / DRQ125[[1, 4]] /. %
```

```
0.564642
```

At this saturation level the inductance loss in negligible.

At 100C, which is the max expected temp, the core loss will probably increase but the allowable margin is ~50%, which may well be adequate.

It really seems like two 6.8μH units in series will work.

All the tries below failed.

API−Devlevan<HCT.pdf>p.1, the HCT−503seems possible. It's surface mount in sort of an undesirable way.

<arnold/coretran.pdf> is a good reference, the whole directory for that matter. See also <ferronics/*>. The <magnetics_inc/> directory is also very informative (e.g. "Inductor Design..." <sr−1a.pdf>).

<coiltronics/DR_Specs−PM−4310.pdf>the DR125 is big enough. It's a shielded bobbin ~1cm.

This sucks. Maybe buy a core?

Note that the '4007 datasheet p.15 mentions that Δi should be < 0.6*iavgmax. This is because the IREV comparator will cut off the current when the reverse current reaches −0.3 × iavgmax (typ,), therefore if the ripple exceeds 0.6*Δiavgmax, the negative current excursion will be clipped, and the charger will not regulate down to zero current.

The constraints on the inductor are

L ≥ 12μH (10μH marginal)
Isat ≥ 6A
Low core loss at 300kHz and full current. (Less than say 250mW?)
Low copper loss at full current. (Less than core loss.)

To figure this we need the Inductance/turns relation. Saturation flux density. Core loss figures @300kHz. Window area and filling fraction. Core to ambient thermal resistance. And that's it.

The industry standard inductance formula is

```
L[μH] -> AL N^2 / 10000 (* AL in μH / 100 t *)
```

Arnold, API−Devlevan,MagneticsInc., TDK, Ferroxcube, EPCOS?

Arnold doesn't make ferrite toroids?
Oh yeah, API isn't a core manufacturer.
ferroxcube selector <http://www.ferroxcube.com/prod/assets/fertor.htm>
power ferrites <http://www.ferroxcube.com/prod/assets/powapp.htm>

For toroid selection, TDK has the skimpy e137.pdf.
MagneticsInc. has a decent catalog <FC−601.pdf>(toroid data on p.139) so at the moment they're ahead. (They also have a sales office in Seattle.) p.6 Recommends Materials F,K,P,R. Looking at p.13 it looks like R−type is the best choice for loss. The Ferroxcube catalog <HB2002.pdf> is also quite good. p.33 offers an f×Bmax graph that suggests 3C96 material would be best (This is not born out by more detailed analysis? Possibly 3F3, 3F35?).

Magnetics offers interpolation parameters for core loss using this equation

```
MagIncCoreLosseq = a * (f / 1000)^c * (B / 1000)^d * 10*^-3;
(* Watts / cm^3 *)
```

Where f is in Hz, B is in Gauss, and the power loss is Watts per cubic centimeter.

Here are the loss parameters for Magnetics materials at 300kHz

```
MagMat = {{"Material", "a", "c", "d"},
          {"F", 0.0573, 1.66, 2.68},
          {"K", 0.00113, 2.19, 3.10},
          {"P", 0.0434, 1.63, 2.62},
          {"R", 0.036, 1.64, 2.68}};
```

```
Magpwr[row_] := {row[[1]], MagIncCoreLosseq /.
    {f → fmax, a → row[[2]], c → row[[3]], d → row[[4]]} /. asu}
```

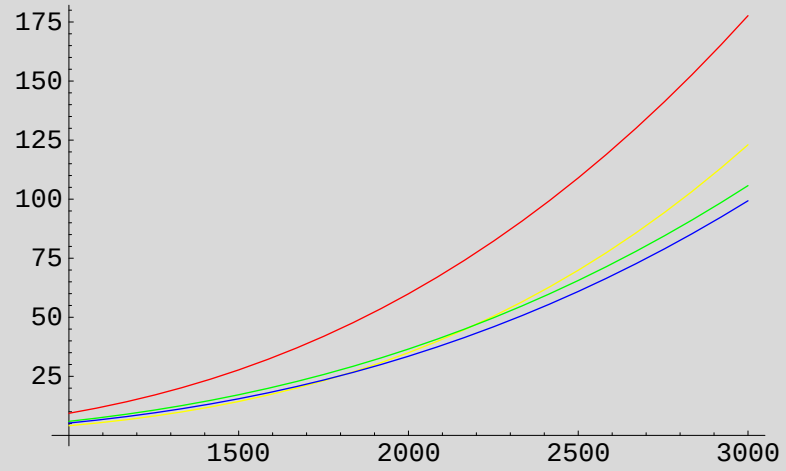
```
Magpwr[MagMat[[3]]]
```

```
{K, 2.04598×10^-9 B^3.1}
```

```
Magpwr /@ Drop[MagMat, 1]
```

```
{{F, 8.52971×10^-8 B^2.68}, {K, 2.04598×10^-9 B^3.1},
 {P, 8.20606×10^-8 B^2.62}, {R, 4.76789×10^-8 B^2.68}}
```

```
Plot[Evaluate[%[[All, 2]]], {B, 1000, 3000},
  PlotStyle → {Hue[0], Hue[1 / 6], Hue[1 / 3], Hue[2 / 3]}];
```



So the F material is ruled out. The R material looks best, but the K material has desirable stability if its lower permeability (about 1/2) can be tolerated.

Following the MagneticsInc. procedure (p.38) Assume 50% winding factor, 500 circular mils per amp.

Use L = 12μH, i = 6A (could use 10/5 but conservative)

Ferroxcube <HB2002.pdf> p.6 gives symbols and units followed by explanations.

Since i can't find decent design info (though i'm sure it's right in front of me) i'll work it out.

```
Lru = (L → AL N^2);
```

For a toroid, Effective Area (Ae) is just Area (A). The minimum area is also equal to (A). The effective length is just the average circumference.

Inductor formula assuming toroids and no air gaps (A in cm^2 and ℓ in cm)

$$L == 0.4\,\pi \times 10^{-8}\,\frac{\mu\, A\, N^2}{\ell}\,[H],\quad B == 0.4\,\pi\,\frac{\mu\, i\, N}{\ell}\,[Gauss],$$

$$H == 0.4\,\pi\, N\, i / \ell\,[Oe],\quad E(*energy*) == \frac{i^2\, L}{2}\,[J],$$

$$Vc == A\,\ell\,(*\ \text{core volume in cm}^3\ *)$$

Must not saturate (B < Bmax), must have minimum inductance. Let k = 4π/10, Let ee = 10E−8

```
NFaradayru = (Solve[B == k μ i N / ℓ, N][[1, 1]])
```

$$N \to \frac{B\,\ell}{i\, k\, \mu}$$

```
L → k ee μ A N^2 / ℓ /. NFaradayru
```

$$L \to \frac{A\, B^2\, ee\, \ell}{i^2\, k\, \mu}$$

```
E == L i^2 / 2 /. % /. {A → Vc / ℓ, B → Bmax}
```

$$E == \frac{Bmax^2\, ee\, Vc}{2\, k\, \mu}$$

```
CoreVolru = (Solve[%, Vc][[1, 1]])
```

$$Vc \to \frac{2\, k\, E\, \mu}{Bmax^2\, ee}$$

So knowing something about the energy stored ($L\, i^2 / 2$) for a given material implies a minimum volume (Vc).

Well, let's try something for materials K, R, 3C96, 3F3, and 3F35. (Note, 1mT = 10 Gauss)

```
Mat = {{"Material", "Perm", "CoreLoss[mW/cm^3]", "Bsat[G]"},
       {"K", 2500, 610, 3950},
       {"R", 4500, 520, 3600},
       {"3C96", 4000, 430, 3700},
       {"3F3", 3250, 400, 3300},
       {"3F35", 1890, 300, 3700}};
```

Permeability @ 1000G, Core loss is @ 300kHz, 100C, 1000G, Bsat is at 100C.

The core loss figures are for sine waves with peak amplitudes of 1000G. The K material seems inferior, otherwise it looks like a trade off between permeability and core loss.

The core loss formula above suggests an approximately 2.6 power law relation between core loss and flux density. In our case we want core losses under 100mW/cm^3, which means a factor of 5 less than the 1000G figures in the "Mat" table. (Note that the tabled losses are for sine wave amplitudes expressed as peak values, i.e. the field excursion is +1000G to −1000G.) To get a factor of 5 reduction with a 2.6 power law, the peak field should be reduced to 1000-G/5^(1/2.6) = 538G. Which is not too bad.

Our targeted current ripple is 0.4*4A = 1.6A, expressed as a peak value this is 0.8A.

MagneticsInc. gives toroid data as AL in mH/1000t, and {a,b,c} = {OD, ID, H} in mm.

Comparing inductance formula

```
Solve[k ee μ A N^2 / ℓ == AL / 1000 (N / 1000)^2, AL][[1, 1]] /.
 {ee → 1*^-8, k → 4 π / 10}
```

$$AL \to \frac{4\,A\,\pi\,\mu}{\ell}$$

Estimate the required core volume for the 3F35 material

```
Vc /. CoreVolru /.
   {k → 4 π / 10, μ → 1890, E → L i^2 / 2, Bmax → 500, ee → 1*^-8} /.
  {i → 6, L → 12*^-6} // N (* cm^3 *)
```

```
410.408
```

Well, that’s wrong.

Try a "big" toroid. (OD, ID, H) = (25.4, 15.5, 10)mm. In R material, AL = 2220[mH/1000t] figuring μ = 2300.

```
Solve[12*^-6 == 2220 / 1000 (N / 1000)^2, N] // N
```

```
{{N → -2.32495}, {N → 2.32495}}
```

Call it 3t

```
2220 / 1000 (N / 1000)^2 /. N → 3 // N // EngineeringForm
```

$$19.98 \times 10^{-6}$$

Basically 20μH.

The current variation contributing to core loss is only 0.8A, see above

```
B → 0.4 π μ i N / ℓ /.
 {μ → 2300, i → 0.8, N → 3, ℓ → π (1.55 + 2.54) / 2} (* Gauss *)
```

```
B → 1079.71
```

We were looking for 500G, but remember, the inductance is increased some too.

```
diLmax /. L → 20*^−6 (* amps *)
```

```
0.980392
```

Iterating this in

```
B → 0.4 π μ i N / ℓ /.
 {μ → 2300, i → % / 2, N → 3, ℓ → π (1.55 + 2.54) / 2} (* Gauss *)
```

```
B → 661.585
```

This is pretty good. Unfortunately, these ferrites saturate at about 3500G, and scaling this to 5A (the max DC current) implies 6600G, which is too much. Try doubling the core volume. (36, 23, 10) AL = 2030

```
2030/1000 (N/1000)^2 /. N → 3 // N // EngineeringForm
```

```
18.27 × 10^−6
```

```
diLmax /. L → 18.3*^−6 (* amps *)
```

```
1.07147
```

```
B → 0.4 π μ i N / ℓ /.
 {μ → 2300, i → 5, N → 3, ℓ → π (3.6 + 2.3) / 2} (* Gauss *)
```

```
B → 4677.97
```

That’s pretty close, but this is a HUGE core. Un−gappedtoroids are just not going to cut it.

Ok, coiltronics DR125 series? <DR_Specs−PM−4310.pdf>
Oops, been updated now DRQ series <DRQ_Specs.pdf>
Anyway, this could really work DRQ125−150in parallel mode (datasheet DRQ_Specs.pdf)

15.35μH @ 0A, 250mVrms
4.27Arms for +40°C conduction loss
5.69A for 30% inductance loss at 20°C
29.8mΩ max @ 20°C

18.4V·μs @ 100kHz for loss equal 10% of loss causing +40°C temperature rise
12.5mm square × 6mm high

Assume the inductance is decreased by the DC current not the AC (a slightly invalid small signal assumption). The inductance at 4A is

```
4 / 5.69
```

```
0.702988
```

From the OCL vs Isat DRQ125 graph the resulting inductance is 97% of the initial value. Conservatively use 95%.

```
0.95 * 15*^-6 (* H *) // EngineeringForm
```

$$14.25 \times 10^{-6}$$

```
diLmax /. L → 14*^-6 (* amps *)
```

```
1.40056
```

Peak current

```
4 + % / 2 (* amps *)
```

```
4.70028
```

Looks good.

The applied Volt*seconds is just Δi * L

```
diLmax * L // EngineeringForm
```

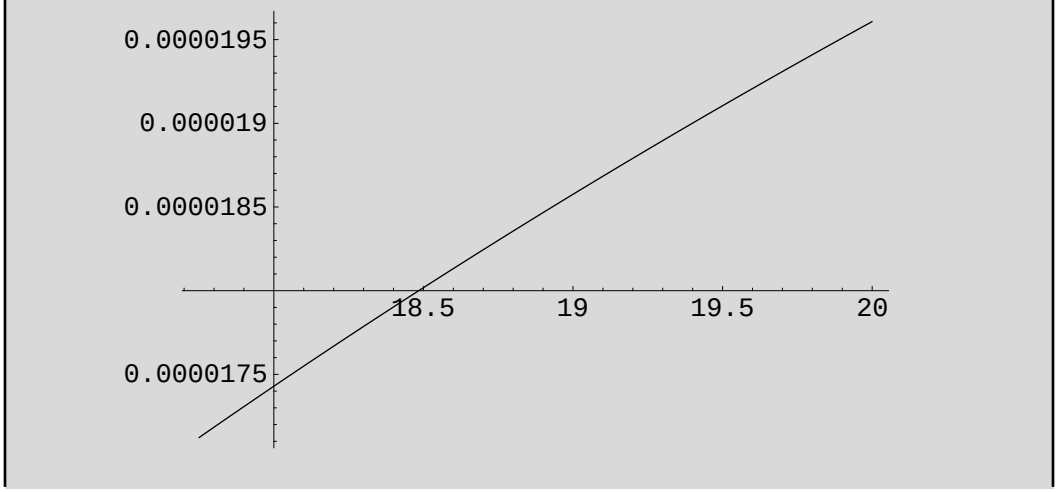
$$19.6078 \times 10^{-6}$$

Better check this. From calculations above, the applied Volt*seconds are

$$\frac{\text{Vbat}\,(\text{Vin} - \text{Vbat})}{\text{f}\,\text{Vin}} \;/.\; \{\text{Vbat} \to \text{vbatmin},\ \text{f} \to \text{fmin}\} \;/.\; \text{asu};$$

This increases with decreasing Vbat. With Vin?

```
Plot[%, {Vin, 17.75, 20}];
```



So the maximum Vs are

```
%% /. Vin → uvmax /. asu // EngineeringForm
```

$$19.6078 \times 10^{-6}$$

This value agrees with the previously calculated value. (Of course the calculation is redundant ;).

Reading the "Irms Derating with Core Loss" graph for 20Vμs, the Vs factor is

```
20 / 18.4 (* 18.4 from the table above *)
```

```
1.08696
```

Call it 109%, the derating is 52% @ 300kHz, meaning the V·s loss will account for 48% of the loss required to raise the temperature +40°C. Since the 100% rated current is 4.27Arms this must be reduced to.

```
4.27 * √0.52 (* amps *)
```

```
3.07914
```

Unfortunately, this is less than the RMS current we are using, so this part is undersized. However, increasing the inductance a little bit while sticking to the same case size would work by cutting the core loss, but two parallel units would be required.

Capacitors(s)

■ C2000
0.1μF, 50V 1206

Input bypass capacitor for low−power battery charger circuitry. This cap. is a common bypass cap. The manufacturer recommends 0.1μF, sounds good. The voltage rating should be 25V minimum. 50V is a much safer choice. Ceramic for low cost and good high frequency performance.

■ C2001a, C2001b
10μF, 50V, Y5V, 1210 muRata 490−1891−−1−ND 1.24/$10

Buck converter input capacitor.

Maximum ripple current is 1/2 load current =~2A . Not a problem for ceramic units. The maximum input voltage (hopefully not including surge).

20uF @ 25V Pan:1210x4 X5R 2.9$; Pan:1812x2 X5R 6.11$; Pan:1210x2 Y5V 2.48$
Mu:1206x4 X7R 2.47$; Mu:1210x2 X5R 3.54$; Mu:1210x2 Y5V 1.93$

20uF @ 50V Pan:1210x2 F 1.52$; Mu:1206x4 Y5V 1,7$; Mu:1210x4 X5R 8.79$
Mu:1210x2 Y5V 2.25$;

The best X5R @ 25V is 1210x2, 3.54$, the best Y5V is 1210x2, 1.93$. So @ 25V, Y5V saves money, but not space.

The best (and only) X5R @ 50V is 1210x4, 8.79$. For Y5V, 1210x2 for 2.25$.

So, if 25V is ok, X5R is the best choice. If 50V is required, the space doubles unless Y5V is used.

Well, estimate the voltage ripple.

```
ΔV → Δi / f C /. {Δi → 2, f → 300*^3, C → 20*^−6} // N
```

```
△V → 0.333333
```

It does seem true that we’d like to hold the ripple no more than this. Allowing 1/2V of miscellaneous loss

```
uvmin − 1 / 2 − vbatmax /. asu
```

```
0.45
```

```
uvnom − 1 / 2 − vbatmax /. asu
```

```
0.7
```

This is on the border line for Y5V, which can loose 60% of it's value when hot. (However the tolerance on the muRata units is +80−20%, so we could still be ok.) If we're careful not to loose more than 1/2V anywhere else, everything should be ok. At worst the umbilical voltage could be bumped to 20V, but that is not desirable, 19V is probably fine.

We could go with 25V, and maybe should, but with transient issues until actual measurements are done, don't do it, stick with 50V.

■ C2002a, C2002b
10μF, 50V, Y5V, 1210 muRata 490−1891−−1−ND 1.24/$10

Buck converter output capacitor.

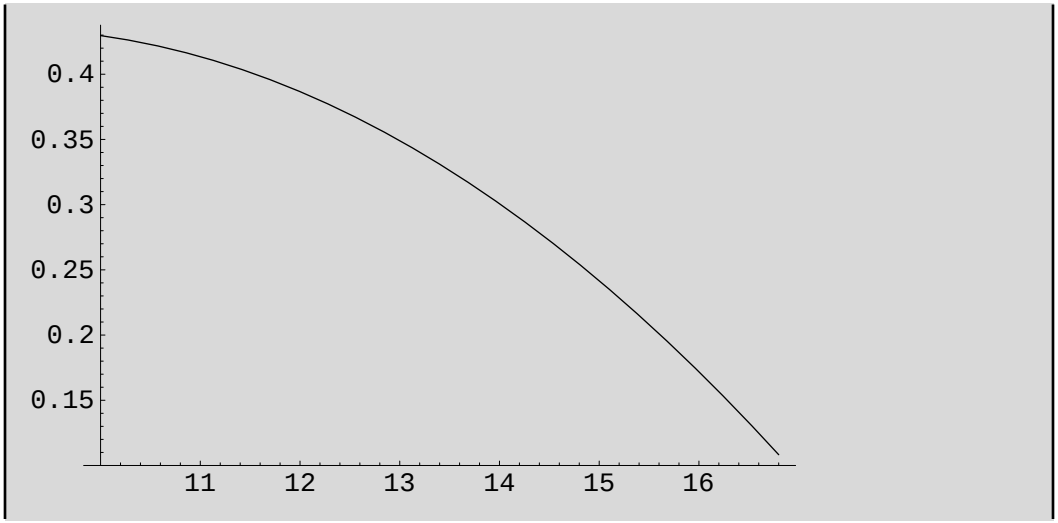
Absorbs the output ripple. This has a lot to do with EMI, but there could be 2nd order efficiency issues. The datasheet gives an RMS ripple current formula

$$\Delta\text{ioutrms} = 0.29\ \text{Vbat}\left(1 - \frac{\text{Vbat}}{\text{Vin}}\right) \Big/ (\text{L f});$$

```
Δioutrms /. {Vin → 18, L → 10*^-6, f → 300*^3}
```

$$0.0966667\left(1 - \frac{\text{Vbat}}{18}\right)\text{Vbat}$$

```
Plot[%, {Vbat, 10, 16.8}];
```



So the ripple increases with decreasing battery voltage. It will also increase with increasing input voltage. The worst case ripple is therefore

```
Δiouteq /. {Vbat → 10, Vin → 20, L → 10*^−6, f → 300*^3} (* amps *)
```

```
0.483333
```

Estimating the ripple voltage

$$\Delta V \to \frac{\Delta i}{f\,C} \;/.\; \{\Delta i \to \%,\ f \to 300*^3,\ C \to 10*^{-}6\}$$

$$\Delta V \to 0.161111$$

It's not that it wouldn't be nice if this was smaller. Of course this is worst case. The data sheet uses 20μF, Ok, spend the 2.25$, and layout two caps. That will get the ripple down to ~80mV. Add some ferrite beads to the output.

■ C2003 0.12μF 1206

Current loop compensation capacitor / Soft−Startcapacitor.

The manufacturer recommends 0.12μF, this is fine unless there is a transient behavior issue. As a soft−start, 0.12μF gives about a 2ms delay (datasheet p.14). This is probably adequate. The plan is to have the PIC hold off the charger anyway. C2003 could be increased solely for soft−start,but that seems risky because of transient issues?

The voltage at ITH is never above 10V.

■ C2004 4.7nF 1206

Low pass filter element for current setting pin "PROG".

The datasheet does not suggest a time constant, however all the examples use

$$f \to \frac{1}{2\,\pi\,R\,C} \;/.\; \{R \to 26.7*^3,\ C \to 4.7*^{-}9\}\ (*\ \text{Hz}\ *)$$

$$f \to 1268.27$$

This is a long time compared to the switching frequency.

```
fnom / f /. % /. asu
```

```
236.543
```

Maintaining the same time constant with R2007 = 30.1k

```
C → 1/(2 π R f) /. %% /. R → 30.1*^3
```

$$C \to 4.1691 \times 10^{-9}$$

No problem sticking with 4.7nF.

■ C2005 15nF 1206

Low pass filter for umbilical current shunt. See R2002.

■ C2006 1μF 1206

Hold capacitor for battery thermistor.

The LTC4007 battery charger chip implements a pulse−basedthermistor measuring scheme. This saves an IC pin at the expense of a larger filter capacitor.

During the first phase of thermistor measurement, the ’4007 NTC pin is driven positive to approximately 4.5V. This state is maintained for the tdrive period. At the end of the drive period, the NTC pin is placed in a high−impedancestate and the voltage across C2206 is measured by the chip. The measurement period is given by tmeasure below, where Rrt is the chip’s master timing resistor R2009.

```
tdriveeq = 127.5 * 20 * Rrt * 17.5*^−12;
```

```
tmeasureeq = 10 * Rrt * 17.5*^−12;
```

The main constraint on C2006 is that the voltage droop during tmeasure not be excessive. During normal operation the ’4007 is either driving the NTC pin to ~4.5V or NTC is briefly disconnected for measurements. Therefore, excluding voltage droop, the voltage on C2006 is always close to the desired voltage across the thermistor.

In this case, the worst voltage droop is when the thermistor is hot. The voltage droop on a capacitor drained by a resistor (R) for time (t) is

```
Vdroop == V0 (1 − Exp[-t/(R C)]) /. {R → R2010 / 7, V0 → Vdrive / 8}
```

$$\text{Vdroop} == \frac{1}{8}\left(1 - e^{-\frac{7\,t}{C\,R2010}}\right) \text{Vdrive}$$

```
Solve[%, C][[1, 1]] // FullSimplify
```

```
Solve::ifun : Inverse functions are
   being used by Solve, so some solutions may not be found.
```

$$C \to -\frac{7\,t}{R2010\,\text{Log}\left[1-\frac{8\,Vdroop}{Vdrive}\right]}$$

Set Vdroop to 10mV

```
% /.
  {Vdroop → 10*^−3, t → tmeasureeq, R2010 → 30.1*^3, Vdrive → 4.5}
 /. Rrt(* See R2009 *) → 453*^3
```

$$C \to 1.02778 \times 10^{-6}$$

So a 1μF capacitor will droop at most about 10mV. This seem fine.

■ C2007
1μF 1206

Low pass filter for umbilical presence detect.

When the umbilical plug is present, the umbilical detect line (the third contact on the umbilical receptacle) is floating. When the umbilical plug is removed, the detect line is connected to the umbilical power negative conductor. Two signals from the PIC, Umbilical_Check (UmbChk), and Umbilical_Detect (UmbDet), monitor the detect line. When detection is enabled, the UmbChk line is brought high, if the umbilical plug is present, C2007 charges to Vdd, otherwise it remains grounded. During a launch, as the rocket leaves the pad, the umbilical is pulled out and the voltage on C2007 rises. Once the voltage crosses the high level input threshold, the PIC detects loss of the umbilical as part of the launch detect decision.

Since the timing of the launch detect is somewhat critical, we want the transition on UmbDet to fairly fast, but not too noisy. As a thought, if τ was around 10ms, the transition should be complete within 3 time constants or about 30ms. If the acceleration was 20gee, in 30ms the rocket would move

```
d → 1/2 a t^2 /. {a → 20 * 10 m/s^2, t → 30*^−3 s} // N
```

$$d \to 0.09\,m$$

That is, about 10cm. That seems about right. If the driving impedance was 10k, the required capacitor is

```
C → t / R /. {R → 10*^3, t → 10*^−3} // N
```

$$C \to 1. \times 10^{-6}$$

Which is right around what we're looking for.

■ C2008 0.1μF, 50V 1206

Bypass capacitor for U2001.

The manufacturer hints (datasheet 4412f.pdf p.7) that bypassing may be required. This cap. is a feel−good value to guard against unlikely stray inductance.

■ C2009 1μF 1206

Low pass filter element for battery voltage measurement.

Really just a noise filter. If R2028 is set to 4.7k, the battery voltage divider impedance is 15k, so total source impedance is 20k. The battery voltage should change only slowly, so a long time constant is ok. Try 100ms.

```
C → 0.1 / 15*^3
```

$$C \to 6.66667 \times 10^{-6}$$

That's a bit large. We are already using 1μF filters on the thermistor. Stick with that and get a ~10ms time constant, which is fine.

■ C2010, C2011 0.1μF, 50V 1206

Input/Output bypass capacitors.

The hope is to minimize the reception and transmission of high frequency noise. The value seems reasonable, the voltage rating a prudent minimum.

■ C2012, C2013, C2014, C2015 ???(~0.01μF???) 1206

Overload response delay capacitors.

The value of these capacitors will depend on the nature of the loads that are powered. However ~1ms delays suggest 0.01μF capacitors. See R2036 for more details.

■ C2016, C2017, C2018, C2019 ???(~0.1μF???) 1206

Soft−Ondelay capacitors. (See also R2042, R2046.)

These capacitors provide the energy storing element for the RC turn on delay circuits provided for each APS output power switch. For various reasons it's convenient to keep the values of the circuit's resistors fixed and control the turn on speed by varying the capacitors.

The theory is very simple. The mosfet turns on when its gate to source voltage reaches the threshold value. Once enhanced sufficiently to carry the initial load current the gate to source voltage remains approximately constant as the gate voltage rises (source follower) until the source voltage nears the drain voltage and the transistor enters saturation.

Using the delay network associated with U2002 as a concrete example, when U2002 begins driving the GATE pin, C2016 charges through R2042 until the voltage on C2016 reaches the mosfet threshold voltage. By this time the GATE pin has reached nearly its final value, in our case probably above 20V. As discussed in its section, R2046 does not greatly effect the timing of the turn on phase.

Once the mosfet reaches threshold and begins to turn on, the voltage across R2042 is equal to (V_GATE −Vthreshold), which we ball−parkestimate as 20V. The initial dV/dt is therefore

```
20/R2042 / C2016 /. R2042 → 100*^3 // N // EngineeringForm (* V/s *)
```

$$\frac{200.\times 10^{-6}}{C2016}$$

Since the FET is acting as a source follower during this phase, the load will experience approximately the same initial slew rate. Of course the slew rate will decrease with increasing gate voltage, but since the GATE pin voltage is considerably above the supply, the voltage vs time is graph is fairly linear compared to the normal RC charging curve.

■ C2020a, C2020b 10μF, 25V, 1210

Filter and hold−upcapacitors for LTC1154 high side drivers. (See also R2030)

At a minimum C2020 must store enough charge to fully turn off all four high side switches.

The total turn off time is on order 100μS. The maximum supply current is around 500μA per driver, so 2mA total. The required charge is

```
2*^-3 * 100*^-6 // N (* Coulombs *) // EngineeringForm
```

$$200.\times 10^{-9}$$

If we allow a 10V drop the required capacitance is

```
% / 10 // EngineeringForm (* Farads *)
```

$$20.\times 10^{-9}$$

This value presents no problem.

The largest convenient capacitor is a 10μF, 25V ceramic unit. Which provides an RC time constant of

```
R2030 * 10*^-6 (* seconds *) /. R2030 → 6.8 // EngineeringForm
```

$$68. \times 10^{-6}$$

This is a bit short. Putting two capacitor in parallel put the time constant over 100μS. In one time constant, the minimum voltage will still be above 5V, so this should work.

Resistors(s)

■ R2000
10Ω 5% 1206

In−rushlimiting, low−passfiltering resistor.

During hot−plug events, prevents DC overshoot to the ’4007. Also forms a low pass filter. The draw on the ’4007 is under 5mA. Assume the target voltage drop is 50mV

```
50*^-3 / 5*^-3
```

```
10
```

A 10Ω resistor might be appropriate. The damping factor must be adequate. The main constraint is the maximum overshoot. We assume an input step function of 20V with the voltage on C2000 = 0V. The maximum voltage allowed on the ’4007’s DCIN pin is 32V, so the max allowable overshoot is 60%. This is good, it sounds nice and high.

The equation for a series LRC circuit in terms of current is

$$i \frac{1}{L C} + i' \frac{R C}{L C} + i'' == 0$$

The generic equation is

$$\omega_n^2 x + 2 \omega_n \zeta x' + x'' == 0$$

Comparing terms

$$\left\{\omega_n \to \frac{1}{\sqrt{L C}}, \zeta \to \frac{1}{2} \frac{R C}{\sqrt{L C}}\right\}$$

The maximum overshoot for an underdamped system ($\zeta < 1$) is given in most introductory control books, i used Kuo, eq.(6-96)

```
FindRoot[0.6 == Exp[-π ζ / Sqrt[1 - ζ^2]], {ζ, .2}]
```

```
{ζ → 0.160493}
```

So a damping ratio over 0.16 is ok

```
Solve[ζ == 1/2 R C / Sqrt[L C], L][[1, 1]]
```

$$L \to \frac{C\,R^2}{4\,\zeta^2}$$

```
% /. {R → 10, C → 0.1*^-6} /. ζ → 0.16 // EngineeringForm
```

$$L \to 97.6563 \times 10^{-6}$$

This means that if the line inductance is less than 100μH, the overshoot will be acceptable. 100μH is quite a lot for stray inductance, even in a long line. The situation is probably further improved by increasing the value of C2000.

■ R2001
20mΩ 1% 100ppm 2512 1W 8.16$/10 P20MCT−ND

Umbilical current shunt resistor

U2000's data sheet 4007f.pdf, Fig.8, p.17 states the current limit will begin when the voltage across R200 is 100mV. So a 5A limit would be

```
0.1 / 5 // N (* Ohms *) // EngineeringForm
```

$$20. \times 10^{-3}$$

The power dissipated is

```
5^2 *% (* W *)
```

```
0.5
```

Which is high enough to worry about.

Select the 1W 2512 from Panasonic

Considering going to 8 amps

Measure the umbilical connector @ 5.84A, got ~0.390V drop. It was pleasantly warm to the touch.

```
5.84 * 0.39 (* Watts *)
```

```
2.2776
```

Power dissipation into the airframe should be excellent. The resistance is

```
0.39 / 5.84 (* Ohms *)
```

```
0.0667808
```

At 8 amps

```
64 * % (* Watts *)
```

```
4.27397
```

I think this is ok, but we need to try it.

Here's what i think. Use 4 x 50mΩ resistors in 1/2W 1812 packages. Use the Stonehenge layout with wide flanges for power dissipation, and wire it either 20mΩ or 12.5mΩ depending on the eventual current target.

■ R2002
5k 5% 1206

Along with C2005, forms an RC filter network for the umbilical current measurement.

The datasheet recommends 5k and 15nF, sounds good. The 3dB frequency is

```
   1
──────── /. {R → 5000, C → 15*^-9} // N // EngineeringForm
2 π R C
(* Hz *)
```

$$2.12207 \times 10^{3}$$

This is well below the switching frequency.

■ R2003
20mΩ 1% 100ppm 2512 1W 8.16$/10 P50NACT−ND

Battery charge current shunt resistor

Since the accuracy of the ’4007 is only about 4% (5% over temperature), errors around 1% over temperature are not significant. A 100ppm resistor over a 100C span is only 1%. 1% initial accuracy also seems adequate.

Something came up sizing the timing resistor, so what’s below was modified. See R2009.

Following the datasheet, set the drop at maximum charge current to 100mV.

```
0.1 / 4 (* Ohms *) // N // EngineeringForm
```

$$25.\times 10^{-3}$$

```
4^2 * % (* Watts *)
```

$$0.4$$

Since DigiKey doesn’t carry 25mΩ 2512’s, make a 25mΩ with 2 x 50mΩ in 1210 size. The overall package will be of similar size, and though the rating is only 1/2W instead of 1W with the 2512, the dissipation can actually be better due to the opportunity for more copper.

Also the errors for resistors in parallel combine using

$$x == f[u, v],\ \sigma_x{}^2 == \sigma_u{}^2 \left(\frac{\partial x}{\partial u}\right)^2 + \sigma_v{}^2 \left(\frac{\partial x}{\partial v}\right)^2$$

Let Rp be the parallel combination of Ra and Rb

$$Rp == \left((Ra \pm \alpha)^{-1} + (Rb \pm \beta)^{-1}\right)^{-1} ==$$
$$\left(\left(\frac{1}{Ra} \pm \frac{\alpha}{Ra^2}\right) + \left(\frac{1}{Rb} \pm \frac{\beta}{Rb^2}\right)\right)^{-1} ==$$
$$\left(\frac{1}{Rp} \pm \sqrt{\frac{\alpha^2}{Ra^4} + \frac{\beta^2}{Rb^4}}\right)^{-1} ==$$
$$Rp \pm Rp^2 \sqrt{\frac{\alpha^2}{Ra^4} + \frac{\beta^2}{Rb^4}}$$

If $\alpha = \beta$, and Ra = Rb, this reduces to

$$\frac{1}{2}\left(Ra \pm \frac{\alpha}{\sqrt{2}}\right)$$

So paralleling resistors improves accuracy as $\sqrt{n}$.

■ R2004
2.94k 1% 1206

Along with R2005, measures voltage across battery charge−currentshunt.

This resistor couples into the current control loop (see U2000). For calculations, see R2009.

■ R2005
3.01k 1% 1206

Battery voltage sense resistor. Fixed current is sunk through this resistor. Apparently to satisfy common mode restrictions of CA1. The resulting voltage drop is compensated if the resistor values is 3.01k, so stick with that.

■ R2006
6k 5% 1206

Part of the current loop compensation. Also sets the gain inside the current loop, which is servoed out.

The manufacturer chooses 6k. Absolutely no known reason to change this unless problems are observed with transient behavior. See also C2003.

■ R2007
30.1k 1% 1206

Current programming resistor.

The value for R2007 was selected in the calculations for R2009 as 30.1k . The target current is 4A .

■ R2008
51.1k 1% 1206

Trickle−currentprogramming resistor.

Seriously discharged batteries are first trickle charged. The target current is C/10 or ~400mA.

```
0.4 == iavgmaxeq /. fixed /.
  {R2003 → 0.02, R2004 → 2940, R2005 → 3010};
```

```
Solve[%, rprog][[1, 1]]
```

```
rprog → 81123.8
```

```
rprog - 30.1*^3 /. %
```

```
51023.8
```

51.1k is plenty close enough. One could argue for 49.9k.

■ R2009
453k 1% 1206

Charge−Timesetting resistor. Minimize stray capacitance.

Recommended value 270k, timing accuracy ±15%

The timer period is given by

```
T → Rrt / 1.54 × 10^5 (* Hours *)
```

This may also be expressed as

```
Tru = (T → 10 * 2^27 * Rrt * 17.5*^-12 (* seconds *));
```

```
1 / (T / (3600 Rrt)) /. Tru
```

```
153269.
```

The range of period expected by the manufacturer is between 1 to 3 hours.

R2009 also influences the drive / measure times of the thermistor network.

```
tdrive → 127.5 * 20 * Rrt * 1.75 × 10^-11
```

```
tmeasure → 10 * Rrt * 1.75 × 10^-11
```

Referring to the "Charge Characteristics" graph on the battery manufacturer's datasheet <DS_BT31930297.pdf> p.2, the total charge time after the current falls to C/10 is about 1 hour. When the '4007 detects C/10, it sets the remaining charge time to 1/4 of the maximum charge time. The total charge time at the C/1 rate from the graph is 3 hours. The 3/4 hour top−offperiod is very close to correct, but may slightly imbalance the pack over time. Although, as pack capacity decreases, this tendency is somewhat self−compensating.

If the charge current measuring shunt can be scaled to the same value as the umbilical measuring shunt (20mΩ) and the FLAG\ threshold reduced to C/20, the 3/4 hour top off would be about right.

Referring to the "Charge Characteristics" graph again, working forwards from the C/20 level, the time to finish charging is about 3/4 hour.

Attempt scaling of rprog

```
Solve[0.05 == rncthc, rprog][[1, 1]]
```

```
rprog → 30442.4
```

With a 20mΩ charge current sense resistor, we would scale the input resistors also

```
iavgmaxeq /. fixed /. R2003 → 0.02 /. R2005 → 3010 /. %
```

```
0.00164244 (−1069.34 + 1.19 R2004)
```

```
Solve[%82 == 4, R2004][[1, 1]]
```

```
− Part::partw : Part 1 of {} does not exist.
```

```
{}[[1, 1]]
```

The closest std. values are 2.94k and 30.1k.

```
rncthc /. rprog → 30.1*^3
```

```
0.0545263
```

```
iavgmaxeq /. fixed /.
 {R2003 → 0.02, R2004 → 2940, R2005 → 3010, rprog → 30.1*^3}
```

```
4.05529
```

This looks pretty good. It justifies a 3 hour time out.

```
3 * 3600 == T /. Tru
```

```
10800 == 0.0234881 Rrt
```

```
Solve[%, Rrt][[1, 1]] // EngineeringForm
```

```
Rrt → 459.807 × 10^3
```

Say next lower std. value (453k)

```
(T /. Tru /. Rrt → 453*^3) / 3600 (* Hours *)
```

```
2.95559
```

■ R2010
30.1k 1% 1206

Drive / Measure resistor for LTC4007 battery−temperaturemeasurement.

See RT100 for explanation.

■ R2011
10k 5% 1206

Protection resistor for umbilical presence detect circuit.

If the PIC connected directly to the umbilical detect line, various nasty things could happen exposing the PIC to excessive voltages and currents. A 10k resistor is small enough that it should not interfere with the measurement of the umbilical detect line, yet it should limit any fault currents to acceptably low values.

■ R2012
10k 5% 1206

Pull up resistor for umbilical presence detect. See C2007 for explanation.

■ R2013
220Ω 5% 1206

Emergency current limiting resistor for Rocket_Ready signal.

If anything "bad" happens, this resistor tries to save our PIC. It should be as large as possible without interfering with the Rocket_Ready signal.

Assume 1V of "margin" desirable. Assume ’HC CMOS logic levels. Minimum at the ground computer is 3.15V. The diode drops 720mV max. Assume 10Ω max for cable resistance, and 4.75V minimum supply,
Vdd−0.7Vminimum output voltage, and 4.7k minimum pull−downresistor.

$$Vground == (Vdd - VPIC - Vdiode)\ \frac{Rpulldown}{Rpulldown + Rcable + R};$$

```
Solve[%, R][[1, 1]] // FullSimplify
```

$$R \to -\frac{\text{Rcable Vground} + \text{Rpulldown}\,(-\text{Vdd} + \text{Vdiode} + \text{Vground} + \text{VPIC})}{\text{Vground}}$$

```
% /. {Vdd → 4.75, VPIC → .7, Vdiode → .72, Vground → 3.15}
 /. {Rpulldown → 4.7*^3, Rcable → 10}
```

$$R \to 258.571$$

Assume that 20mA is bad for the PIC, R = 220Ω would protect against voltages up to

```
20*^-3 * 220 // N
```

```
4.4
```

Admittedly this isn't a very high voltage. Still, it's better than nothing.

■ R2014, R2015, R2016, R2017, R2018, R2019, R2020 47k 5% 1206

Pull up resistors for LTC4007 digital I/O lines.

In some cases (e.g. FLAG\) the pull up resistor is present to translate the voltages used by the '4007 to those used by the PIC. When used as a voltage translator, the '4007 output is open−collector.The pull up is connected to the PIC's Vdd supply, thus bringing the line up to Vdd when the '4007's output is de−asserted.

In other cases (e.g. EN\) the pull up brings a signal into the '4007 to a valid logic state even if the PIC, for any reason, sets it's output line to a high impedance state (always the case immediately after power−onreset).

The pull up values used here are project−widestandards, supposedly a compromise between noise immunity and power consumption.

■ R2021 Eliminated v0.5

Pull up resistor turning off Q2003. (Q2003 has been eliminated.)

■ R2022, R2023, R2024, R2025 10k 5% 1206

Paranoia resistors for high side drive inputs.

These resistors are questionable. If the supply polarity was reversed they would limit current into the PIC, but everything would be pretty much destroyed at that point anyway. A possible use would be limiting current flow in the event

of voltage breakdown in the high side drivers. This is a very serious fault, but it is possible and these resistors might save the PIC in this circumstance.

These probably could be 47k, but 10k seems more conservative. The voltage drop is negligible, so only noise immunity really matters. 10k is plenty of current limit.

■ R2026, R2027, R2028, R2029 10k 5% 1206

Paranoia resistors for high side drive status outputs.

Also see the comments for R2022.

These resistors are less convenient than R2022, etc., because they force fairly high value for the pull up resistors R2050−2053,but that's ok. I just wonder if these are necessary.

■ R2030 6.2Ω 1206

The no−blow−upno−stay−onresistor. (See also C2020)

There are two functions fulfilled by R2030. The first involves the voltage rating of the LTC1154s. They are rated 18V maximum operating voltage, and we are running them at 18V. Therefore we want no power glitches. To this end R2030 acts as a low pass filter.

As a further complication, if a short circuit on an output line were to bring the bus voltage below the minimum operating voltage of the '1154s, which is 3.5V, they would not be able to turn off the output FETs and interrupt the short, probably destroying something.

The solution to both these problems is to use the largest R and C possible and affordable.

The R value (R2030) is limited mostly by the voltage drop. Any voltage drop across R2030 subtracts from the current sensing shunt voltages. For this reason the drop on R2030 has been somewhat arbitrarily limited to 10% of the current limit threshold voltage of 100mV. Since the typical quiescent draw of the '1154 at 18V is 400μA, and there are 4 units, the maximum resistor is

```
10*^-3/(4*400*^-6)//N
```

```
6.25
```

There is some risk that the current draw could be considerably higher than calculated here due to manufacturing variation. In the worst case the drop would be about a factor of 2 greater, but this is very unlikely, and not fatal. Note however that the supply current rises with decreasing temperature. Which means the current limit will rise by as much as 10% as the temperature decreases to −25C.This seems ok.

■ R2031 Not Installed

Extra resistor for complex thermistor circuit. Presently not used, see RT100.

■ R2032, R2033, R2034, R2035 ???(shunts) 2512

Output current measuring shunts.

The outputs of the APS are protected against over−currents by monitoring the voltage across these shunts. When the voltage across the shunt reaches 100mv±25% and sustains this voltage for a minimum time set by other circuit components, The affected output is shutdown until reset by microprocessor command.

The maximum DC current for each output is about 6A (See Q2006). The required shunt is

```
.1 / 6 // N (* Ohms *) // EngineeringForm
```

16.6667×10^{-3}

The maximum power dissipation in the shunt during steady state is

```
0.125^2 / % (* Watts *)
```

0.9375

Probably we won't ever run this much current through one output. However a 1W resistor is still prudent. The 2512 size will handle 1W and the 2512 pad can be arranged so that 1206 and greater packages may be soldered into the same location.

For common load currents the shunt values are

```
{0.1 / {4, 3, 2, 1, 0.5}} (* Ohms *) // MatrixForm
```

(0.025 0.0333333 0.05 0.1 0.2)

The corresponding dissipations are

```
0.01 / % (* Watts *) // MatrixForm
```

(0.4 0.3 0.2 0.1 0.05)

Note, that since there is some voltage drop across R2030 (typically 10mV) The actual trip currents will tend to be about 10% higher than calculated, but this is effect is still smaller than the ±25% accuracy of the LTC1154.

■ R2036, R2037, R2038, R2039 ???(~100k???) 1206

These resistors, along with capacitors C2012−C2015 form 4 separate delay networks. Each network filters the current−sense signal for one of the APS output power switches. By adding delay to the current−sense signal brief overloads are prevented from tripping the over−current protection and shutting down the load. Once tripped, a load's power switch must be reset by the APS−PIC before power to the load is restored.

Sizing the over−current delay involved at least 3 considerations. One is the power source, which is often a Li+ battery pack. Normally we do not want a single load fault to bring the battery voltage below the minimum required to operate the system, which suggests a fairly brief delay. Also the output switch itself is an N−channel mosfet and is subject to safe operating area constraints. Finally, most often, the actual load will set the most stringent overload protection requirements.

The actual delay before a load is shut off is a function of both the RC delay and the magnitude of the overload. The LTC1154 datasheet <lt1154.pdf> fig.5 p.9, provides a graph showing the shutdown time in RC−time−constant units as a function of overload magnitude.

The actual values for these resistors requires knowledge of the load characteristics. However, ~1ms delays are reasonable. A 100k resistor and 0.01μF capacitor are reasonable starting points.

■ R2040, R2041 47k 5% 1206

Pull up resistors for battery charge counter signals.

Speed is not a big issue since the falling edge is what counts. Use our rocket−standard 47k.

■ R2042, R2043, R2044, R2045 100k 5% 1206

Turn on delay resistors.

Certain loads, particularly those with large input capacitors, draw several times their steady state current when first switched on. Since our output power switches are high speed solid state devices, (which we like). There is a possibility that certain loads would trip the over−current protection during start up. To prevent this each high side output driver's gate pin drives an RC filter which slows the voltage rise on the output transistor's gate thus limiting the turn−on speed of the output,

The LTC1154 datasheet says that the part can turn on an IRLZ24 in about 100μs. The IRLZ24 has a total gate charge of around 20nC, so the '1154 is sourcing about

```
20*^-9/100*^-6 (* amps *) // N // EngineeringForm
```

$$200.\times 10^{-6}$$

The datasheet indicates this is correct for 18V drive, see the "Gate Drive Current" graph p.5.

After subtracting the mosfet threshold voltage ~(2−5)V there is a maximum of about 20V to drive a resistor such as R2042. To keep the draw under 200μA the maximum value is

```
20 / % (* Ohms *) // EngineeringForm
```

$100. \times 10^{3}$

In fact this value isn't really marginal because the voltages aren't really reaching 20V during turn on and it's not that critical, and also the datasheet uses this value, so fine.

The only reason noticed to change this value would be to reduce the size of the delay capacitor if it were to become inconveniently large.

■ R2046, R2047, R2048, R2049 100k 5% 1206

Gate damping resistor.

When the soft−on circuit (see R2042, C2016) is used these resistors connect the mosfet gate to the delay capacitor. Connecting a mosfet gate directly to a capacitor driven by a high impedance will typically cause oscillations because of the Miller capacitance. This resistor prevents those oscillations by forcing the transition−inducedcurrents from the FET to the delay capacitor to be small.

The interesting question at the moment is what value of resistor should be used here? Often with high impedance FET drivers a value of 1k is used. In fact a Linear Technologies application note on high side drivers (an−53.pdf, p.3) suggests exactly that value. On the other hand, every other example in the app.note and in the LTC1154's datasheet use a 100k resistor. Since there is no explanation anywhere for this, we will now make one up.

Experience and reason suggest that 1k is sufficient to prevent oscillations. There is no particular reason to believe that 100k would be harmful, except of course that it will slow the rate of turn on. However, the whole point of the soft−on circuit is to retard the turn on rate, so that's not really bad. A typical FET from the datasheet has a total gate charge around 20V of 20nC. This is sort of equivalent to a 1nF capacitor. The typical delay capacitors (See C2016) are running more than 100 times this value. Therefore we expect, if the two resistors for example R2042 and R2026, have the same value, that the delay capacitor will dominate the turn on timing.

So far all this merely suggests that a 100k damping resistor is not a bad thing. The question remains why use such a large value. The answer is probably found during the turn off phase. During turn off the '1154 must sink current to discharge the FET gate, and also any current coming through the damping resistor. If the damping resistor was only 1k, and the delay capacitor charged to 20V, the initial current would be 20mA. This is probably beyond what the '1154 will sink, and is anyway unnecessary because as we have seen a 100k resistor is usable.

Another possible benefit of a large damping resistor is softening turn on in the event of rapid power cycling. Although a small resistor would actually discharge the delay capacitor faster, if not fully discharged, a large resistor will limit the speed that the output can rise. By the same token, it is wise to wait a minimum time before re−enabling a soft started load so that the delay capacitor will really be discharged. About 150ms per μF of delay capacitance might be about right. For this reason, using a resistor larger than about 100k is not advisable.

Anyway, 100k is fine.

■ R2050, R2051, R2052, R2053 120k 5% 1206

Pull up resistors for output power switch status lines.

Theses pull ups are required since the status lines are open collector. If the 10k series resistors are used (see R2026) than these pull−ups must be large enough to meet minimum logic requirements. LTC1154 Vstatus_max is 0.4V at 400μA. PIC input low is 0.9V max @ 1μA.

The easy way (figure 0.45V for noise immunity)

```
Solve[0.45 == (5 - 0.4) 10*^3/(R2060 + 10*^3) + 0.4, R2060][[1, 1]]

R2060 → 910000.
```

So 100k would probably work. The LTC1154 datasheet uses 120k, who are we to argue?

■ R2054
30.1k 1% 1206

Drive / Measure resistor for PIC battery−temperaturemeasurement.

This resistor exists because of the pulse measurement scheme used by the LTC4007 (see C2006 for further explanation). When the ’4007 is operating, the voltage on C2006 is always about equal to the voltage expected for an ordinary thermistor voltage divider. In this case R2027 merely functions as an inconveniently large series resistor between the capacitor C2006 and the PIC A/D pin. (The large value may necessitate extra waiting during the acquisition phase of the A/D conversion cycle in the PIC.) When the ’4007 is shut down, it has been assumed that the NTC pin acts like a high impedance. The PIC may therefore continue to measure the battery temperature by first driving the thermistor network through R2027, and then quickly measuring the resulting voltage on C2006 in a manner almost identical to that of the ’4007 itself.

In fact the behavior of the NTC pin on the ’4007 during shutdown is not documented AFAIK, so the behavior may be different than assumed. Even if this is so, as long as the behavior is consistent, such as a diode drop or current sink to ground, useful temperature measurements can still be made, we hope.

The value of this resistor is somewhat arbitrary. A case could be made for using a value that was more convenient for the PIC measurements. A 10k would not require delay during the acquisition phase, and might be more convenient otherwise, however it seems simpler to try to match the voltage vs temperature characteristics of the thermistor network when read by the ’4007 or the PIC as closely as possible. With this in mind the value here is chosen to be the same as that of the other thermistor resistor, R2010.

■ R2055
4.7k 5% 1206

Paranoia resistor for battery voltage measurement.

Really can’t think why this is needed, but the source impedance is already 15k, so a 4.7k is no big deal.

Miscellaneous

- **E2000, E2001, E2002**
  DN470xCT−ND(SMB2.5−x)(p.675)